Development of Reflow Fill of CGeSbTe Films for Sub-20 nm Cells in 3D Cross-Point Memory

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To obtain reliable and scalable cells in 3D cross-point memory, endurance failures caused by voiding from etching damage to memory cells should be resolved to preserve the properties of GeSbTe (GST) phase-change materials. Herein, the fabrication of a damascene cell without patterning, which relies on the bottom-up fill of carbon-doped GST layers into confined cells, is proposed as a promising solution. The reflow fill of the sputtered carbon-doped GST films into confined cells at high-temperature and low-power conditions is demonstrated, and a mechanism in which Sb and Te transfer into the cell through vapor transfer and viscous flow due to capillary pressure is verified. The aspect ratio increases from 2 to 7.7 under enhanced vaporization of Sb and Te as well as the capillary force. The advanced reflow-fill process using a laser can overcome the limit of the conventional reflow-fill technology by increasing the atomic mobility above the melting temperature. Based on the proposed method, 19 nm cross-point memory devices are successfully integrated together with the Ovonyx threshold switch and appropriate memory windows are secured. Furthermore, the 9 nm cells exhibit reliable endurance cycles over 10⁸.

1. Introduction

Dynamic random access memory (DRAM), flash memory, and logic devices have played an important role in providing storage solutions to meet the data explosion avalanche of recent decades. However, due to the fundamental limitation of charge loss with scaling,^[1] DRAM requires a suitable large-charge capacitor, and flash has to resolve serious issues such as the maintenance of coupling between the control and floating gates, stress-induced current leakage, and cell-to-cell parasitic interference between the stored charges.^[2–6]

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To continually develop large-scale and high-performance devices for exploding data needs in the internet of things, cloud services, and big-data storages, entirely new approaches to resistance memories such as magnetic memory, phase-change memory, and resistive memory not based on charge should be tried and realized. Among these approaches, GeSbTe (GST)based phase-change memory has been a candidate due to better endurance cycles and scalability, longer data retention time, individual bit addressability, higher productivity, and lower cost from small cell area (4 F²) compared to DRAM (6-8 F²).^[7-13]

Intel and Micron announced 128 Gb of 3D cross-point memory in July 2015^[14] for boosting the operation speed of high-capacity memory or enabling fast mass data transfer between input and output operations. Intel renamed 3D cross-point memory as "Optane" and released it in

products,^[15] including a cache card (M.2 format, 32 GB) and an solid state drive (SSD) (PCIe format, 375 GB).

When users select the Optane cache card, the input/output (I/O) speed of a personal computer can be enhanced close to the I/O speed of pure SSD storage through combination with hard disk drive (HDD) storage at the lower price of 22–40%. This is because the Optane cache card accelerates the I/O speed of conventional HDDs by ≈14 times. In addition, the Optane SSD (Optane DC P4800X) can achieve a read/write latency under ≈10 µs, which is approximately ten times faster than a conventional flash SSD.

However, the present 3D cross-point memory has critical drawbacks such as scalability and reliability issues because it is based on the characteristics of GST phase-change materials. Void formation in the device is well known as one of the most fatal failures in endurance tests, and is caused by Joule heating during amorphous-to-crystalline transitions of GST materials, and vice versa.^[9,16–18] The electrical break between the heater and phase-change layers due to the voids results in a significant high resistance that is not controllable by input pulsing.

The void formation can be prompted by several causes, such as the density difference between amorphous and crystalline states during cycling,^[19] electromigration by electrostatic forces,^[20,21] coalescence of microvoids and vacancies,^[22] and volatile species from etching-gas reactions.^[23] With regard to





Figure 1. TEM images of a) standard, b) small, and c) misaligned cell after reset programming, and d) endurance failure cell after 5 × 10⁵ cycles.

microvoids and vacancies, an endurance failure due to etch chemistry will be more severe than one due to another cause, since the damage layer is directly exposed to the program volume (PV) of GST phase-change materials in a 3D crosspoint memory cell.

For reliable applications of 3D cross-point memory devices that require a larger endurance cycle of over 10^{8} ,^[15] an alternative solution to cell patterning should be considered to suppress the voids because of etch damaging to the phase-change layer.^[24,25]

As an alternative to cell patterning to overcome such drawbacks, we demonstrate a damascene cell without direct exposure to etch chemistry in a 3D cross-point memory cell; thus, a reflow fill of sputtered carbon-doped GST (CGST) films in confined cells rather than chemical vapor deposition of GST films with high impurities for sub-20 nm cells in 3D cross-point memory devices is introduced and suggested.

2. Results and Discussion

2.1. Chemical Etchant Damage to Memory Cells

To find out etchant damages, a 82 nm line-type Phase Change Memory (PCM) device with ring-shaped bottom electrode contact (BEC) was fabricated. Tungsten plugs and CoSix were used as contact materials for bottom electrodes and Si diode, respectively. Word line and bit line were employed for the selection of each cell. For patterning, an undoped silica glass film served as a hard mark to etch TiN/CGST patterns after lithography. As in HBr etching, a 45HBr + 5CF₄ + 50Ar mixing gas was utilized as the HBr etchant.

Figure 1 shows transmission electron microscopy (TEM) images of patterned GST and endurance failure cells after reset programming and 5×10^5 cycles, respectively. Since the PV can be damaged by etching in a small cell size (Figure 1b) and miss aligned BEC (Figure 1c), the patterned cross-memory cells can lead to an endurance failure, as indicated in Figure 1d, which can limit the use of the devices with scaling.

Damascene and patterned planar cells employing 15 at% carbon-doped $Ge_2Sb_3Te_5$ phase-change materials were fabricated for lifetime comparison by programming energy. As

shown in **Figure 2**, damascene cells have a longer lifetime cycle than that of patterned planar cells by as much as two orders of magnitude at a 58 nm storage node based on programming energy. Moreover, the difference increases with scaling by up to three orders of magnitude at a 19 nm storage node. As indicated by a red point in Figure 2, the lifetime cycles of a cell realized by benchmarking^[15] showed fewer life cycles (10⁵ cycles) than expected.

To verify the increased endurance gap between damascene and patterned cells, thermal simulations for each cell were performed with a 2D calculation grid using computational fluid dynamics (CFD-ACE+, ESI Group, France) based on the finite-element method.^[26,27] As described by the simulation and as shown in **Figure 3**a,b, the PV of a patterned GST cell can be damaged by chemical etching because of direct exposure to etch gases, such as HBr, that can easily penetrate the GST cells and generate volatile composites like GeBr₄ and SbBr₃.^[23] In contrast, the PV of a damascene cell has a gap above the upper damaged layer, in which the penetration of etch-gas elements such as H and Br is reduced so as not to reach the PV.



Figure 2. Lifetime time variations with programming energies for different structures of GST cells.





Figure 3. Thermal simulation data of a) 19 nm patterned and b) damascene cells and the location of the damaged layer and program volume.

2.2. Findings of a Reflow Fill of CGST Films

To obtain damage-free PV in GST cells, many researchers have tried to realize a damascene cell by sputter-filling into confined cells without etching processes. We here propose a reflow fill by sputtering processes as given in **Figure 4**a (see Figure 4b for comparison with sputtering fill). When the working pressure, deposition rate, and substrate temperature were changed from 5 mTorr/10 nm s⁻¹/220 °C to 1 mTorr/0.3 nm s⁻¹/280 °C the bottom-up fill (BUF) thickness of the cell increased dramatically from 17 to 78 nm. CGST phase-change layers were deposited on the confined cells with an increase in the film thickness to observe the phenomenon of reflow fill in detail. As shown in **Figure 5**a–c, BUF thickness linearly increases with deposition thickness, but Figure 5d,e shows that the BUF thickness abruptly increases enough to fill confined cells, suggesting that this phenomenon has a different mechanism than a sputtering fill.

2.3. Demonstration of a Reflow-Fill Mechanism

To describe the fill mechanism, as shown in **Figure 6**a, we suggest an Sb/Te transfer model by the capillary pressure caused by the curvature of the confined cell. Evaporation due to the lower heat of Sb and Te vaporization, and viscous flow of GST material by thermal energy are responsible for this mechanism.^[22,28] The rate of initial neck growth between two particles



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Figure 4. SEM images of CGST films of damascene cells with a) reflow fill ($1 \text{ mTorr}/0.3 \text{ nm s}^{-1}/280 \,^{\circ}\text{C}$) and b) sputtering fill ($5 \text{ mTorr}/10 \text{ nm s}^{-1}/220 \,^{\circ}\text{C}$).

with a shape similar to the BUF of a confined cell can be modeled as follows $\ensuremath{^{[29]}}$

$$x = \sqrt{\left(\frac{3\gamma}{2\eta}\right)rt} \tag{1}$$

where γ is the surface energy, η is the viscosity, r is the radius of curvature, and t is the time. In this equation, the driving force originates from the difference in surface curvature between ρ and r as shown in Figure 6a. As the spheres begin to coalesce, the neck has a curvature radius ρ that remains small compared with the surface curvature of the particles r, resulting in a negative pressure that induces the viscous flow of material toward the confined region. Instead of undoped GST films that have a crystallization temperature below 428 K,^[30] the CGST target was used to suppress the growth of



Figure 5. SEM images of confined cells at different thickness of CGST films: a) 15 nm, b) 30 nm, c) 50 nm, d) 100 nm, and e) 125 nm.



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Figure 6. a) Schematic diagram of reflow-fill mechanism by Sb, Te elements transfer based on capillary pressure and viscous flow of CGST materials. b) SEM image of grain growth on the confined cell using undoped GST materials.

GST material by increasing the crystallization temperature of GST films during the deposition to 553 K, because the grown grain can shadow the deposition of sputtered atoms on the bottom of damascene cells, resulting in voiding as shown in Figure 6b.^[31]

To verify the mechanism suggested above, high-resolution TEM images and energy-dispersive spectroscopy (EDS) depth and transversal profilings of the cells were analyzed. The results are shown in Figure 7 and Table 1. The Sb + Te compositions of the BUF area (a) were higher than those of the shoulder area (d), which indicates material transfer by vapor and viscous flow.^[25] As expected, the crystallinity of the BUF area differed from the shoulder area. The BUF area was more crystallized than the shoulder area due to the increased Sb + Te and the relatively decreased C + Ge because the Sb-richer phase has lower crystallization temperatures.^[32] The EDS transversal profiling of elements in the cell exhibits a higher Ge composition in the shoulder area compared to BUF area, as shown in Figure 7f. However, the EDS depth profiling of elements in the BUF area was uniform throughout the thickness range due to the lower heat of vaporization energy of Sb and Te to the case of Ge elements as given in Figure 7e.^[22,33]

Based on Equation (1), the substrate temperature and deposition rate were varied and treated as process parameters because they relate to η and *t*. Figure 8 shows the aspect ratios (ARs) of the SiO₂ mold height to bottom size depending on η and *t*. The increase and decrease of reflow-fill AR with the substrate temperature and deposition rate, respectively, support the suggested mechanism explaining the reflow fill of CGST films. A graph with a drastic increase in the AR from 2 to 7 and TEM images at each position are shown on the left and right sides of Figure 8.

The reflow-fill mechanism distinguishes three regions with BUF thickness variations depending on the top thickness of the CGST films in the confined cells, as shown in **Figure 9** (scanning electron microscope (SEM) images of the same are shown in Figure 5). In the initiation state, the normal sputtering process of metal films occurs, which is named I) sputtering. After the increase in film thickness leading to the vaporization of Sb and Te materials, the vapor flow is dominant in the second state, which is called II) vapor transfer. In the third state, a large capillary pressure on the bottom of the confined cell causes the viscous flow of CGST material toward the bottom of the confined cell due to the lower glass transition temperature.^[34] The third state is called III) viscous flow. Hereinafter, this fill phenomenon is referred to as a conventional reflow fill.

2.4. An Advanced Reflow Fill Using Pulse Laser

The conventional reflow fill is limited by composition change and heater temperature nonuniformity due to vaporization of volatile elements such as Sb and Te. In addition, at temperatures above the crystallization temperature (over 330 °C), surface defects such as abnormal crystal growth can occur. Furthermore, the vaporization and the diffusion of Sb and Te elements are highly dependent on the angle from the horizontal plane to the vertical slope, which can cause large voids (for the cells with greater than 87 °C) due to the lower viscous force by the limited heater temperature, as shown in Figure 11b.

In order to overcome these drawbacks and maximize the viscous flow of CGST films, we developed an advanced reflow-fill technique using a pulse laser to increase the AR without voids. A laser with a wavelength of 515–532 nm (bandgap \cong 2.4 eV) was selected. This is wider than the GST bandgap (0.5-0.7 eV) and wide enough to absorb laser energy. It is also appropriate because the absorption coefficient of GST is highest around the bandgap of 2-3 eV.^[35] Conversely, an appropriate discrete dwell time can be estimated from atomic mobility. To this end, we calculated the element-wise diffusion length of CGST through ab initio molecular dynamics (AIMD) simulations. The AIMD simulations were performed with the Vienna Ab initio Simulation Package (VASP Software GmbH, Austria),^[36] and the Perdew-Burke-Ernzerhof functional was used for the exchange-correlation energies.^[37] The energy cutoff was selected at 350 eV and the k-point in the Brillouin zone was sampled at point Γ . The simulation cell contained 230 atoms (42 Ge, 70 Sb, 88 Te, and 30 C atoms) with the same composition as the experiment, and a simulation trajectory was generated in





Figure 7. a–d) High-resolution TEM images of confined cell by deposited by reflow-fill process and crystallinity at each points of (*a*), (*b*), (*c*), and (*d*). e,f) TEM–EDS depth profiling and transversal profiling of elements at lines of the BUF area.

the canonical ensemble. The initial structures were obtained by randomly distributing atoms and heating at 2000 K for 5 ps to erase nonphysical order. Thereafter, the structures were equilibrated for 70 ps at 900, 1000, 1100, or 1200 K, and the last 20 ps trajectories were sampled to calculate the atomic mobility properties.

The mean square displacement (MSD) is expressed as

$$MSD = \langle R^{2}(t) \rangle = \frac{1}{N} \langle \sum_{i=1}^{N} |R_{i}(t) - R_{i}(0)|^{2} \rangle$$
(2)

Table 1. GeSbTe composition ratios of the confined cell at (*a*) and (*d*) positions by TEM–EDS analyses compared to those of blanket CGST films.

	(a)	(<i>d</i>)	Blanket
Ge (at%)	12	19	21
Sb (at%)	36	35	35
Te (at%)	52	46	44

where R_i represents the coordinates of atom *i*, and *N* the number of atoms in the simulation cell. Based on the calculated MSD, the diffusion coefficient (*D*) and diffusion length (*L*) were obtained by

$$D = \frac{1}{6} \frac{\partial}{\partial t} \lim_{t \to \infty} \text{MSD}(t)$$
(3)

$$L = \sqrt{D \cdot t} \tag{4}$$

Based on the computed D, it is expected that all atoms moved by tens of nanometers around the melting temperature of 900 K during 1 µs (see Figure 10). Accordingly, the dwell time for maximizing laser reflow in the CGST film was estimated to be several hundred nanoseconds. The laser reflow windows were evaluated in reference to a void-free damascene CGST cell. The energy density in Equation (5) and dwell time were varied, as shown in Figure 11a

Energydensity
$$(J \text{ cm}^{-2}) = \frac{\text{Pulse energy}}{\text{Laser beam area}}$$
 (5)





Figure 8. a-c) Reflow-fill aspect ratio of confined cells depending on deposition rate and substrate temperature and high-resolution TEM images of the cells at each point.

For filling of the cells with higher AR (over 5) and vertical slope (greater than 87 °C), the process window is the shaded area between E_{\min} and E_{\max} , in which CGST films fill without voids in the damascene, as shown Figure 11d. For these experiments, C15 (Ge2Sb4Te4) materials were used. When the pulse laser had a high energy density enough to vaporize CGST films, it made an ablation on the surface by the vaporization of Sb and Te elements, which have a lower heat of vaporization.^[22,28] If the energy density of the pulsed laser was low as shown in ^① of Figure 11a, a large void was observed below the middle of the damascene cell, as shown in Figure 11b. As the laser energy density increased, as shown in ⁽²⁾ of Figure 11a, the size of voids reduced by reflow fill was eventually removed in the cells, as shown in Figure 11c,d. Due to a higher laser energy than in the case of conventional reflow fill, the GeSbTe composition ratios of top [®]/middle [©]/bottom [@] in BUF area in the cell are close to that of CGST film, as shown in Table 2, while in the case of conventional reflow fill, Sb + Te composition ratio is rich as shown in Table 1. In addition, the smooth surface of the CGST film was also obtained by advanced reflow filling using a pulsed



Figure 9. BUF thickness variations depending on the top thickness of the CGST films.

laser. This is due to the high diffusion of the elements due to the higher laser energy compared to conventional reflow fills using heating energy.

2.5. Integration and Operation of 19 nm 3D Cross-Point Memory Devices

Cross-memory devices were successfully integrated using reflow fill of CGST films as shown in Figure 12. Cell over peri (COP) scheme was used to increase the cell area for the given die size. The CGST films were deposited on isolated confined cells and separated by the chemical and mechanical polishing (CMP) process. For the self-aligned process, the recess of the top region of the GST cell was carried out by the etch-back process with dilute HBr gas. A TiN top electrode employing a metalorganic precursor was deposited at 543 K by an atomic layer deposition process to avoid vaporization of the GST materials. The confined cells were separated by the CMP process for the self-aligned top electrode. Ovonyx threshold switch (OTS) layers employing SiGeAsTe material were deposited by sputtering on the top electrode and patterned with isolated mask layers. A bit line was formed on the GST/OTS cell, and normal metal line processes were utilized to measure the electrical properties of the GST/OTS cells. Figure 13 shows the distributions of 64 kb sampling for a 1 Gb cell array. For the basic operation of this cell array, we refer to Kim and Lee.^[38] An appropriate memory window between reset and set states by programming operation was obtained up to 1.2 V, which is similar to typical windows from GST operations. Finally, we confirmed that the 1 Gb cell array using damascene cells based on the proposed reflow-fill technology was fully operational, making it a strong contender for next-generation cell technologies.

2.6. Feasibility of Highly Scalable Sub-10 nm Cells Using a Reflow Fill

The sub-10 nm damascene cells were also feasible in the present reflow-fill technology, as shown in **Figure 14**a. Down to 9 nm, the damascene cell operated with resistance differences over one order between set and reset programming. For a







Figure 10. Calculated element-wise diffusion length of CGST materials for 1 µs as a function of temperature.

reset current below 60 μ A, controlling the small contact area to bottom electrode and resistivity of the electrode materials was more effective than the same for GST materials. Furthermore, over 10⁸ endurance cycles were performed in 9 nm damascene cells. As a result, a scalable damascene cell employing the present reflow-fill technology is suggested as a very promising candidate for forthcoming 3D cross-point memory cells. **Table 2.** GeSbTe composition ratios of confined cell by laser reflow fill at position @, @, @, @, and @ of Figure 11d.

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Ge (at%)	19	19	21	22
Sb (at%)	38	38	42	40
Te (at%)	42	42	37	38

3. Conclusion

Findings of reflow fill of CGST films and their basic principle were suggested for sub-20 nm cells of 3D cross-point memory devices. The proven mechanism of Sb and Te material transfer into the confined cell without grain growth of the GST layers by increasing the substrate temperature and decreasing the deposition rate, resulted in a dramatic enhancement of AR from 2 to 7.7 for completing the fill. The fill process can be categorized into normal sputtering, vapor transfer, and viscous flow regions depending on the BUF thickness to the top thickness of the CGST films. For the advanced reflow fill, a pulse laser was employed, and the regimes of CGST reflow with energy and dwell time were classified as void, full fill, and ablation. A voidfree fill window was obtained at a microsecond discrete dwell time based on the calculated diffusion length of CGST. Consequently, the proposed reflow-fill technology makes it possible to fabricate a 19 nm cross-point memory device with an ovonyx



Figure 11. a) Process window as a function of dwell time versus energy density. b–d) TEM images of damascene cells depending on different energy density of \mathbb{O} , \mathbb{O} , and \mathbb{O} at same dwell time.





Figure 12. TEM images of a 19 nm cross-point memory device and cells employing the reflow-fill process.

threshold switch for 1 Gb cell density, and to make a scalable damascene cell to 9 nm with the reflow fill. The life cycle of the devices after patterning was dramatically enhanced, with over 10^8 cycles of write endurance possible.



Figure 13. Distributions of 64 kbit sampling for 1 Gbit cell array depending on set and reset programming, respectively.

4. Experimental Section

15 at% carbon-doped $Ge_2Sb_3Te_5$ thin films with a thickness of 100 nm were deposited on 300 mm Si (100) substrates by increasing the temperature from 513 to 593 K and decreasing the pressure from 0.3 to 0.05 mTorr by Ar gas flow control. A GST single target using a pulsed-DC magnetron sputtering system was employed for this deposition. Several trench patterned cells with different ARs were prepared for reflow-fill demonstration and evaluation according to experimental conditions. For the advanced reflow fill, a pulse laser with wavelengths of 515 and 532 nm, diode, and Nd:YAG (neodymium-doped yttrium-aluminum garnet; Nd:Y₃Al₅O₁₂) source was adopted with a pulse width of 10–600 ns, a beam size of $x = 30 \ \mu m$ to 10 mm and $y = 1-10 \ mm$, a scan speed of 15-100 mm s⁻¹, a frequency of 4-10 kHz, and an energy density of 0.1-10 | cm⁻². After CGST films were deposited on the patterned wafer, the wafer was transferred to the laser system and scanned by pulse laser during incremental movements along the x-axis. The scanned area was overlapped by 50 μ m along the y-axis due to the laser power gradient at the edge of the beam. The overlap size was decided through specific laser power testing and was controlled in accordance with device characteristics.

TEM analyses of cross sections of the trench cell and device were carried out, and EDS measurements were also performed to detect the compositions of the CGST materials.

To evaluate the electrical characteristics, an Agilent 4072 RF pulse measuring system with a pulse generation system was used to measure the reset current, reset/set resistance, and endurance cycles. A square-shaped current pulse was applied to the devices, and the amplitude and width of the current were varied to program the reset and set states.



(c) **(b) (a)** Reset Reset Set 10 Resistance (Ω) 10 Resistance (Ω) 31.48nm 32.46nm 10⁶ 10⁶ _____ 10^t 10 20nm 0 20 40 60 80 100 120 $10^2 \ 10^3 \ 10^4 \ 10^5 \ 10^6 \ 10^7 \ 10^8 \ 10^9$ 10° 10¹ Reset current(uA) Endurance (cycles)

Figure 14. a) TEM image, b) resistance variations with set/reset currents, and c) endurance cycles of a 9 nm damascene cell.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

cross-point memory, damascene, etching damage, fill, GeSbTe, laser, reflow

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- K. Kim, G. Jeong, in *Electronic Device Architectures for the Nano-CMOS Era* (Ed: S. Deleonibus), Jenny Stanford Publishing, Singapore, 2009, p. 187.
- [2] J. A. Mandelman, R. H. Dennard, G. B. Bronner, J. K. DeBrosse, R. Divakaruni, Y. Li, C. J. Radens, *IBM J. Res. Dev.* 2002, 46, 187.
- [3] S. Lai, T. Lowrey, IEEE Int. Electron Devices Meet., Tech. Dig. 2001, 803, 36.5.1.
- [4] K. Kim, S. Y. Lee, Microelectron. Eng. 2007, 84, 1976.
- [5] K. Prall, in 2007 22nd IEEE Non-Volatile Semiconductor Memory Workshop, IEEE, Piscataway, NJ 2007, pp. 5–10.
- [6] S. K. Lai, IBM J. Res. Dev. 2008, 52, 529.
- [7] S. Hudgens, B. Johnson, MRS Bull. 2004, 29, 829.
- [8] S. Raoux, G. W. Burr, M. J. Breitwisch, C. T. Rettner, Y. C. Chen, R. M. Shelby, M. Salinga, D. Krebs, S.-H. Chen, H.-L. Lung, C. H. Lam, *IBM J. Res. Dev.* 2008, *52*, 465.

- [9] A. L. Lacaita, A. Redaelli, Microelectron. Eng. 2013, 109, 351.
- [10] I. S. Kim, S. L. Cho, D. H. Im, E. H. Cho, D. H. Kim, G. H. Oh, C. H. Chung, in VLSI Technology (VLSIT) Symp., IEEE, Piscataway, NJ 2010, pp. 203–204.

www.advmattechnol.de

- [11] M. J. Kang, T. J. Park, Y. W. Kwon, D. H. Ahn, Y. S. Kang, H. Jeong, H. K. Kang, in 2011 Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2011, pp. 3.1.1–3.1.4.
- [12] F. Xiong, M. H. Bae, Y. Dai, A. D. Liao, A. Behnam, E. A. Carrion, S. Hong, D. Ielmini, E. Pop, *Nano Lett.* **2013**, *13*, 464.
- [13] J. Liang, R. G. D. Jeyasingh, H. Chen, H.-S. P. Wong, IEEE Trans. Electron Devices 2012, 59, 1155.
- [14] U. D. Dadmal, R. S. Vinkare, P. G. Kaushik, S. A. Mishra, Int. J. Electron., Commun. Soft Comput. Sci. Eng. 2017, 13.
- [15] U. Pirzada, Intel Developer Forum 2016. "Intel Reveals Optane Technology Brand, '3D XPoint' Based SSDs Coming in 2016 – Upto 7.2x Times The IOPs Performance of Conventional SSDs", Vancouver, British Columbia 2016.
- [16] C. F. Chen, A. Schrott, M. H. Lee, S. Raoux, Y. H. Shih, M. Breitwisch, R. Cheek, in 2009 IEEE Int. Memory Workshop, IMW, IEEE, Piscataway, NJ 2009, pp. 1–2.
- [17] B. Gleixner, F. Pellizzer, R. Bez, in Non-Volatile Memory Technology Symp. (NVMTS), 2009 10th Annual, IEEE, Piscataway, NJ 2009, pp. 7–11.
- [18] A. Padilla, G. W. Burr, K. Virwani, A. Debunne, C. T. Rettner, T. Topuria, R. M. Shelby, in *Electron. Devices Meeting (IEDM)*, IEEE, Piscataway, NJ **2010**, pp. 29.4.1–29.4.4.
- [19] K. Do, D. Lee, D. H. Ko, H. Sohn, M. H. Cho, Electrochem. Solid-State Lett. 2010, 13, H284.
- [20] T.-Y. Yang, J.-Y. Cho, Y.-J. Park, Y.-C. Joo, Acta Mater. 2012, 60, 2021.
- [21] Y. C. Joo, T. Y. Yang, J. Y. Cho, Y. J. Park, J. Korean Ceram. Soc. 2012, 49, 43.
- [22] J. H. Park, S. W. Kim, J. H. Kim, D. H. Ko, Z. Wu, D. Ahn, D. H. Ahn, J. M. Lee, S. B. Kang, S. Y. Choi, *AIP Adv.* **2016**, *6*, 025013.
- [23] J. H. Park, J. H. Kim, D.-H. Ko, Z. Wu, D. H. Ahn, S. O. Park, K. H. Hwang, *Thin Solid Films* **2016**, 616, 502.
- [24] S. L. Cho, J. H. Yi, Y. H. Ha, B. J. Kuh, C. M. Lee, J. H. Park, S. O. Park, inVLSI Technology, 2005. Digest of Technical Papers Symp. on, IEEE, Piscataway, NJ 2005, pp. 96–97.
- [25] J. H. Park, J. H. Kim, D.-H. Ko, Z. Wu, D. H. Ahn, S. O. Park, K. H. Hwang, *Thin Solid Films* **2017**, 634, 141.
- [26] Y. T. Kim, K. H. Lee, W. Y. Chung, T. K. Kim, Y. K. Park, J. T. Kong, in Simulation of Semiconductor Processes and Devices. SISPAD 2003. Int. Conf. on, IEEE, Piscataway, NJ 2003, pp. 211–214.

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- [27] Y. Kim, Y. Hwang, K. Lee, S. Lee, C. Jeong, S. Ahn, F. Yeung, G. Koh, H. Jeong, W. Chung, T. Kim, Y. Park, K. Kim, J. Kong, Jpn. J. Appl. Phys. 2005, 44, 2701.
- [28] B. Chen, G. H. ten Brink, G. Palasantzas, B. J. Kooi, J. Phys. Chem. C 2017, 121, 8569.
- [29] Y. M. Chiang, D. P. Birnie, W. D. Kingery, in *Physical Ceramics*, Wiley, New York, NY **1997**, p. 101 (Ch 2).
- [30] S. Raoux, J. L. Jordan-Sweet, A. J. Kellock, J. Appl. Phys. 2008, 103, 114310.
- [31] J. H. Park, S.-W. Kim, J. H. Kim, Z. Wu, S. L. Cho, D. Ahn, D. H. Ahn, J. M. Lee, S. U. Nam, D.-H. Ko, J. Appl. Phys. 2015, 117, 115703.
- [32] N. Yamada, E. Ohno, N. Akahira, K. Nishiuchi, K. Nagata, M. Takao, Jpn. J. Appl. Phys. 1987, 26, 61.
- [33] J. B. Park, G. S. Park, H. S. Baik, J. H. Lee, H. S. Jeong, K. N. Kim, J. Electrochem. Soc. 2007, 154, H139.
- [34] Z. Sun, J. Zhou, R. Ahuja, Phys. Rev. Lett. 2007, 98, 055505.
- [35] T. Tsafack, E. Piccinini, B.-S. Lee, E. Pop, M. Rudan, J. App. Phys. 2011, 110, 063716.
- [36] G. Kresse, J. Furthmüller, Comput. Mater. Sci. 1996, 6, 15.
- [37] J. P. Perdew, K. Burke, M. Ernzerhof, Phys. Rev. Lett. **1996**, 77, 3865.
- [38] T. Kim, S. Lee, IEEE Trans. Electron Devices 2020, 67.4, 1394.