

Supporting Information

Material Design of New p-Type Tin Oxselenide Semiconductor through Valence Band Engineering and Its Device Application

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1. Cross-sectional SEM images of the SnO film with different oxygen partial pressure

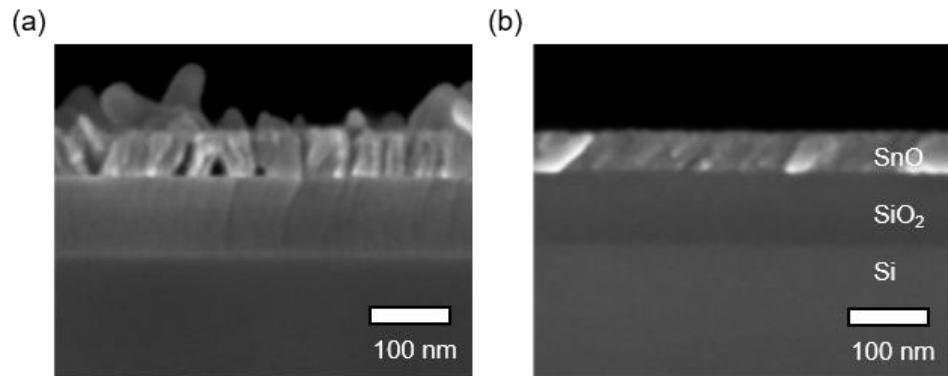


Figure S1. SEM micrographs of the annealed SnO films, which was grown at the oxygen partial pressure of (a) 4 % (left) and (b) 10 % (right) on SiO₂/Si substrates.

2. Plan-view TEM image of the SnSe_{0.56}O_{0.44} film.

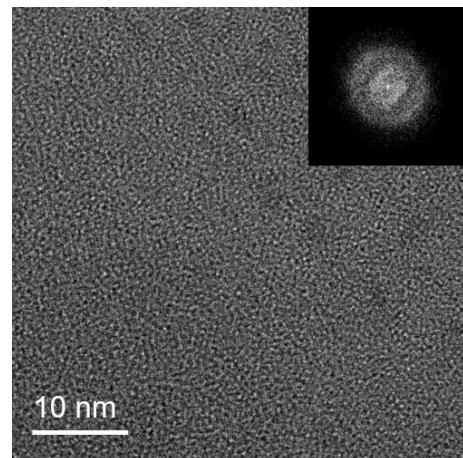


Figure S2. Plan-view TEM image of the SnSe_{0.56}O_{0.44} film. The SADP of the SnSe_{0.56}O_{0.44} film was shown as an inset, indicating the amorphous phase nature.

3. XPS Analysis of the Se 3d peak.

The following deconvolution of the XP spectra of selenium *3d* was based on the ref. 1.

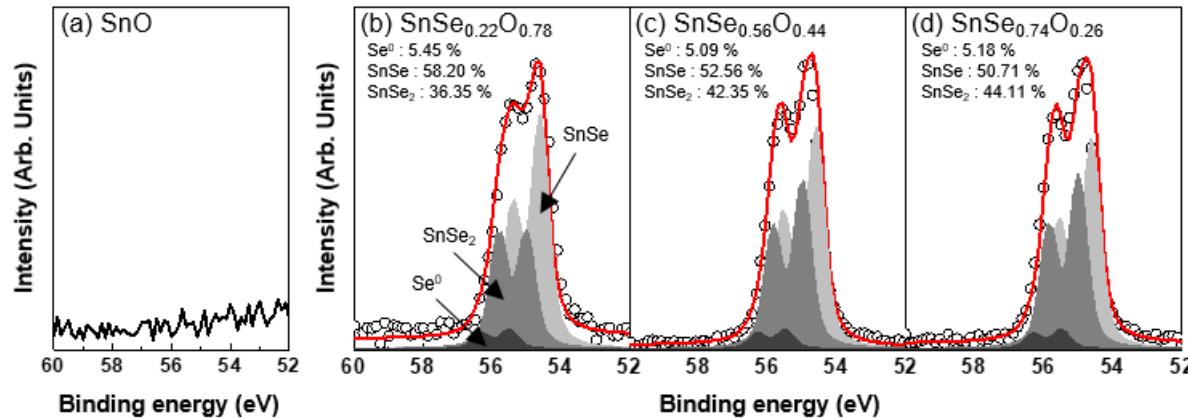


Figure S3. XP spectra of Se 3d of (a) SnO, (b) $\text{SnSe}_{0.22}\text{O}_{0.78}$, (c) $\text{SnSe}_{0.56}\text{O}_{0.44}$ and (d) $\text{SnSe}_{0.74}\text{O}_{0.26}$ thin-films annealed at 300 °C. The binding energy states of the Se with three different bonds (SnSe , SnSe_2 , and Se^0) corresponds to the peaks approximately 54.6, 55.0, and 55.5 eV, respectively.

4. Transmittance and band alignment of the $\text{SnSe}_x\text{O}_{1-x}$ films.

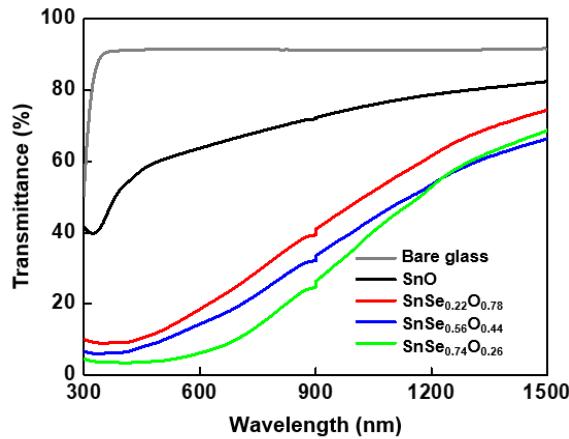


Figure S4. Transmittance of the 30 nm $\text{SnSe}_x\text{O}_{1-x}$ ($x = 0, 0.22, 0.56, 0.74$) thin films annealed at 300 C°.

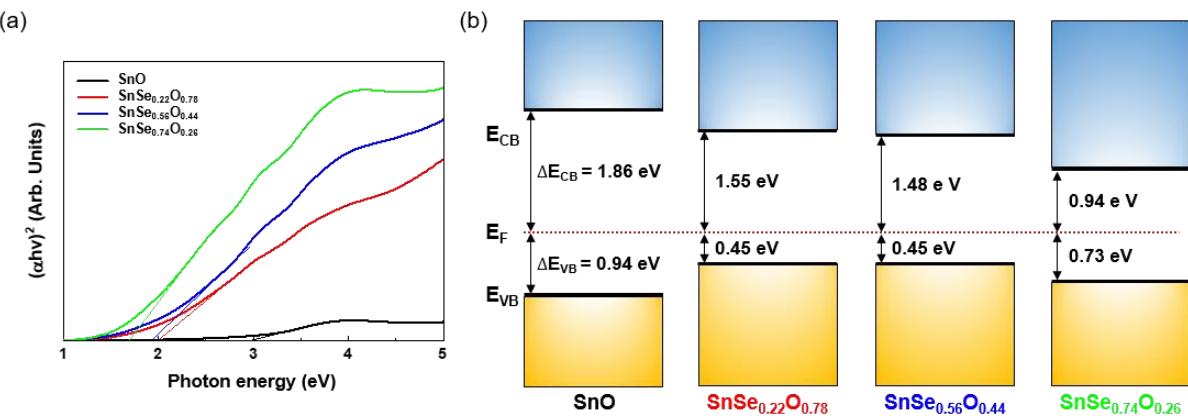


Figure S5. (a) Direct bandgap extracted from the absorption coefficient relative to the photon energy. (b) Band alignment of the $\text{SnSe}_x\text{O}_{1-x}$ ($x = 0, 0.22, 0.56, 0.74$) thin film.

5. I_{DS} - V_{GS} curve and V_{GS} -dependent field-effect mobility variation of the $\text{SnSe}_{0.56}\text{O}_{0.44}$ FETs.

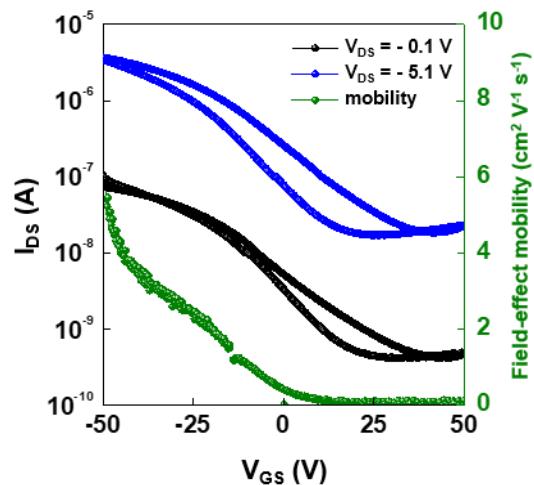


Figure S6. Transfer characteristics and variation in V_{GS} -dependent mobility of the $\text{SnSe}_{0.56}\text{O}_{0.44}$ FETs. I_{DS} - V_{GS} curves were measured in double-sweep gate voltage mode.

6. Electrical characteristics of the $\text{SnSe}_x\text{O}_{1-x}$ films and their FETs near $x = 0.56$.

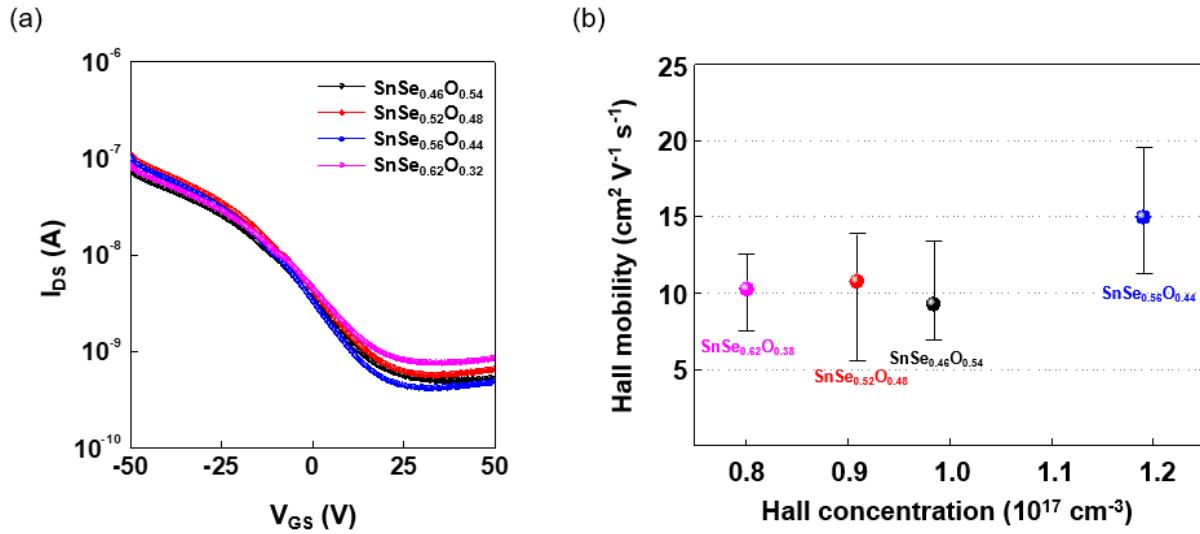


Figure S7. (a) Transfer characteristics of $\text{SnSe}_x\text{O}_{1-x}$ FETs with the Se fraction near $x = 0.56$. (b) Hall effect measurement of $\text{SnSe}_x\text{O}_{1-x}$ thin-films with the Se fraction near $x = 0.56$.

Table S1. Electrical parameters of the $\text{SnSe}_x\text{O}_{1-x}$ films and their FETs with Se fraction near $x = 0.56$.

	$\text{SnSe}_{0.46}\text{O}_{0.54}$	$\text{SnSe}_{0.52}\text{O}_{0.48}$	$\text{SnSe}_{0.56}\text{O}_{0.44}$	$\text{SnSe}_{0.62}\text{O}_{0.38}$
n_h [cm^{-3}]	9.8×10^{16}	9.1×10^{16}	1.2×10^{17}	8.0×10^{16}
μ_{Hall} [$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$]	9.3 ± 2	10.8 ± 3	15.0 ± 4	10.3 ± 3
$I_{\text{ON/OFF}}$	2×10^2	2×10^2	3×10^2	1×10^2
μ_{FE} [$\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$]	4.0	5.3	5.9	4.6

7. Comparison with several important p-type materials recently reported.

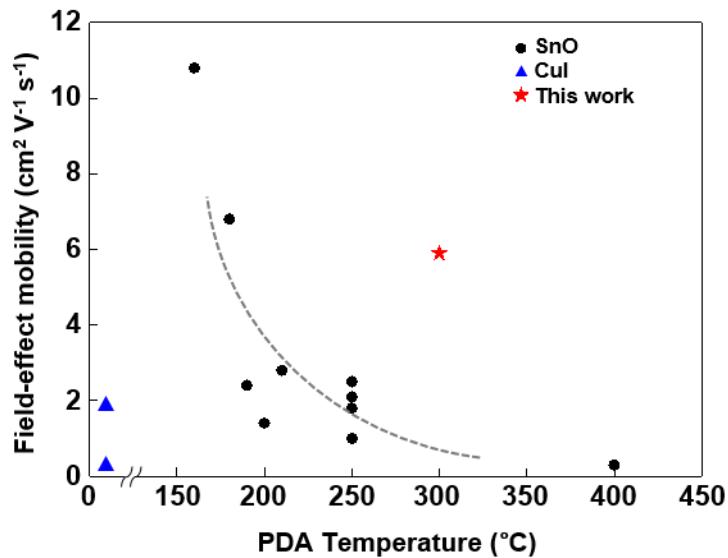


Figure S8. Relation between PDA temperature and field-effect mobility for the high performance p-type SnO FETs, which was summarized from the **Table S2**. It includes the results for the solution-based CuI FETs, which were reported very recently. Most of high performance SnO FETs have been fabricated at $T_{\text{PDA}} \leq 250$ °C.

Table S2. Summary of performance of several important tin monoxide films and related FETs. The recently reported CuSnI and CuI thin film properties were also included.

Gate Insulator ^(a)	Method ^(b)		T _{dep} ^(c) [°C]	T _{PDA} ^(d) [°C]	PDA time [min]	μ _{Hall} [cm ² V ⁻¹ s ⁻¹]	n _h [cm ⁻³]	μ _{FE} [cm ² V ⁻¹ s ⁻¹]	Year	Ref
SnO	SiO ₂	EBE	RT	400	10	-	-	0.3	2012	[2]
SnO	SiO ₂	EBE	RT	400	10	-	-	0.3	2012	[3]
SnO	SiO ₂	RFMS	RT	250	60	3	1.0 × 10 ¹⁸	1.8	2013	[4]
SnO	HfO ₂	DCMS	RT	160	30	-	-	10.8	2013	[5]
SnO	HfO ₂	DCMS	RT	180	30	18.7	2.2 × 10 ¹⁷	6.8	2013	[6]
SnO	YSZ	PLD	575	-	-	7	1.0 × 10 ¹⁷	-	2013	[7]
SnO	HfO ₂	RFMS	RT	250	60	-	-	2.1	2014	[8]
SnO	SiO _x	RFMS	90	-	-	-	-	4.9	2014	[9]
SnO	SiO ₂	RFMS	RT	200	120	1.4	7.0 × 10 ¹⁷	1.4	2014	[10]
SnO	SiO ₂	PLD	500	-	-	2	9.0 × 10 ¹⁶	0.3	2015	[11]
SnO	ATO	DCMS	RT	190	30	-	-	2.4	2015	[12]
SnO	SiO ₂	RFMS	RT	250	100 sec	-	-	1.8	2015	[13]
SnO	SiO ₂	DCMS	RT	210	60	5.5	1.8 × 10 ¹⁸	2.8	2016	[14]
SnO	SiO ₂	ALD	210	250	60	-	-	1.0	2017	[15]
SnO	ZrO ₂	DCMS	RT	250	60	-	-	2.5	2017	[16]
SnO	Al ₂ O ₃	TE	250	-	-	-	-	1.4	2018	[17]
CuSnI	PET	SC	140	-	-	8.9	4.0 × 10 ¹⁸	-	2018	[18]
CuI	SiO ₂	SC	RT	-	-	5.1	5.0 × 10 ¹⁹	0.44	2018	[19]
CuI	ZrO ₂	SC	RT	-	-	5.1	5.0 × 10 ¹⁹	1.9	2018	[19]
SnSeO	SiO ₂	DCMS	RT	300	60	15.0	1.2 × 10 ¹⁷	5.9	2019	This work

- (a) Gate Insulator: Gate insulator used in the Hall measurement or FETs. (YSZ: yttria stabilized zirconia. ATO: superlattice of TiO₂ and Al₂O₃); (b) Method: the deposition method for the channel layer. (EBE: electron-beam evaporation. RFMS: radio-frequency magnetron sputtering. DCMS: direct current magnetron sputtering. PLD: pulsed laser deposition. ALD: atomic layer deposition. TE: thermal evaporation. SC: spin coating); (c) T_{dep} and (d) T_{PDA}: temperature during the deposition and post deposition annealing process, respectively.

8. Comparison of thermal stability between the SnO and SnSe_{0.56}O_{0.44} FETs.

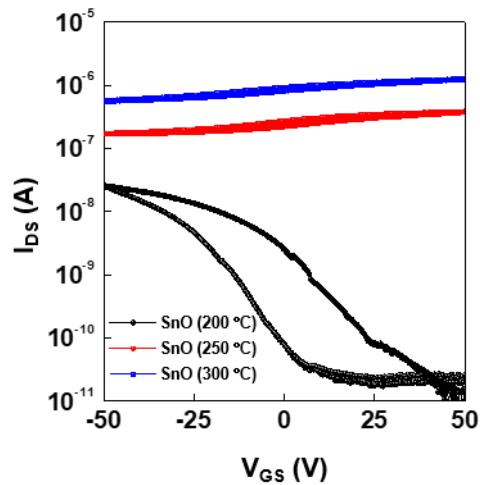


Figure S9. Transfer characteristics of the SnO FETs annealed at different temperatures of 200, 250 and 300 °C. I_{DS} - V_{GS} curves were measured at $V_{DS} = -0.1$ V.

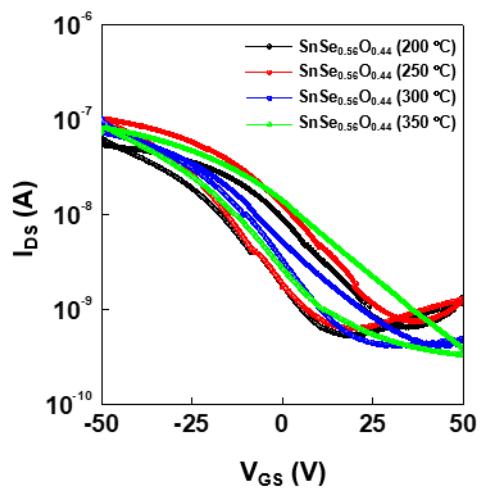


Figure S10. Transfer characteristics of the SnSe_{0.56}O_{0.44} FETs annealed at different temperatures (200, 250, 300 and 350 °C). I_{DS} - V_{GS} curves were measured at $V_{DS} = -0.1$ V.

9. Transfer characteristics of the n-type IGZO FETs for CMOS inverter.

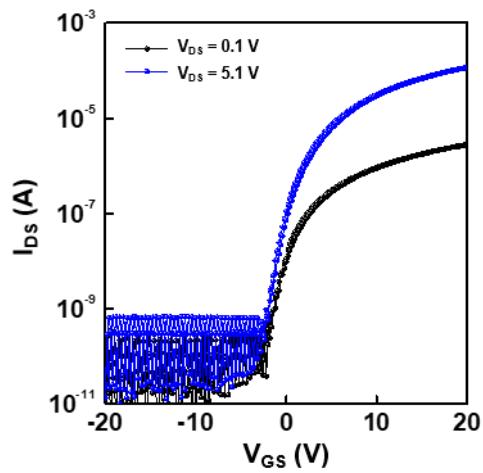


Figure S11. Transfer characteristics of the n-type IGZO FETs adopted for the complementary metal oxide semiconductors.

10. I_{DS} - V_{GS} curves of the $\text{SnSe}_x\text{O}_{1-x}$ FETs in double-sweep gate voltage mode.

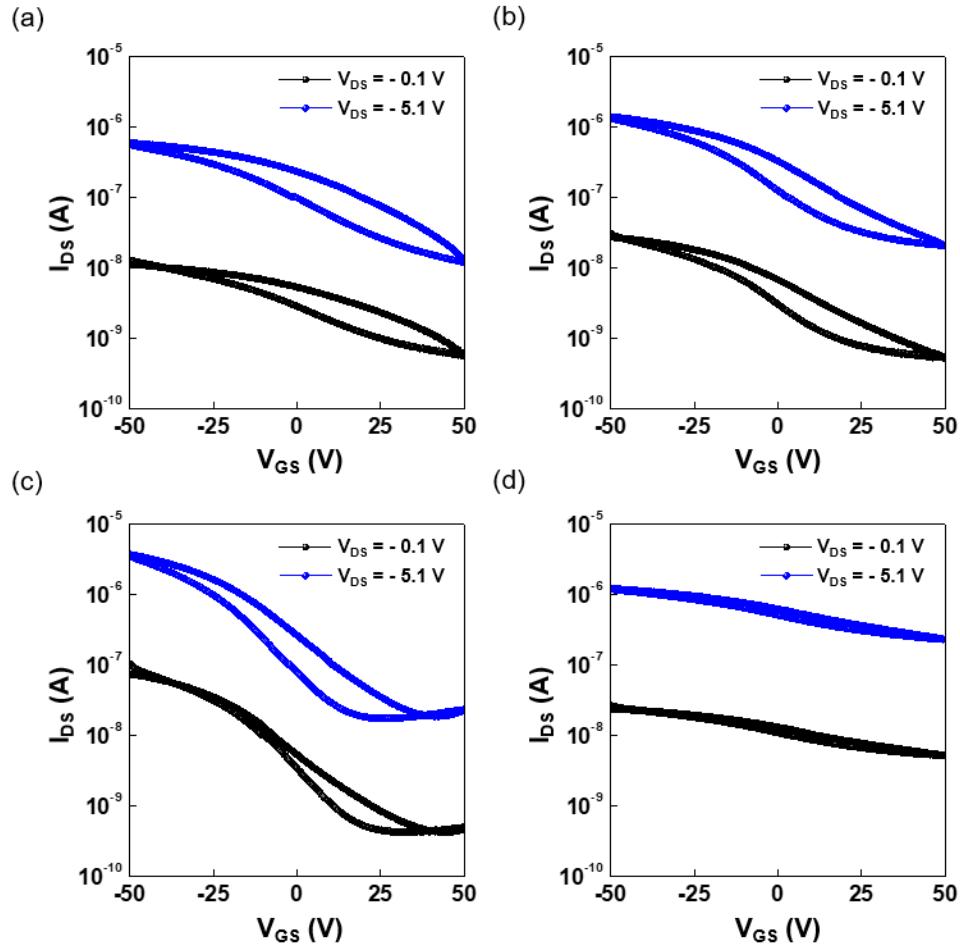


Figure S12. Transfer characteristics of the (a) control SnO, (b) $\text{SnSe}_{0.22}\text{O}_{0.78}$, (c) $\text{SnSe}_{0.56}\text{O}_{0.44}$ and (d) $\text{SnSe}_{0.74}\text{O}_{0.26}$ FETs annealed at 300 °C, which were measured in double-sweep gate voltage mode.

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