Capacitors with an Equivalent Oxide Thickness of <0.5 nm for Nanoscale Electronic Semiconductor Memory

By *Seong Keun Kim, Sang Woon Lee, Jeong Hwan Han, Bora Lee, Seungwu Han,* and *Cheol Seong Hwang**

The recent progress in the metal-insulator-metal (MIM) capacitor technology is reviewed in terms of the materials and processes mostly for dynamic random access memory (DRAM) applications. As TiN/ZrO_2-Al_2O_3-ZrO_2/TiN (ZAZ) type DRAM capacitors approach their technical limits, there has been renewed interest in the perovskite $SrTiO_3$, which has a dielectric constant of >100, even at a thickness ~10 nm. However, there are many technical challenges to overcome before this type of MIM capacitor can be used in mass-production compatible processes despite the large advancements in atomic layer deposition (ALD) technology over the past decade. In the mean time, rutile structure TiO_2 and Al-doped TiO_2 films might find space to fill the gap between ZAZ and $SrTiO_3$ MIM capacitors due to their exceptionally high dielectric constant among binary oxides. Achieving a uniform and dense rutile structure is the key technology for the TiO_2-based dielectrics, which depends on having a dense, uniform and smooth RuO_2 layer as bottom electrode. Although the Ru (and RuO_2) layers grown by ALD using metal-organic precursors are promising, recent technological breakthroughs using the RuO_4 precursor made a thin, uniform, and denser Ru and RuO_2 layer on a TiN electrode. A minimum equivalent oxide thickness as small as 0.45 nm with a low enough leakage current was confirmed, even in laboratory scale experiments. The bulk dielectric constant of ALD $SrTiO_3$ films, grown at 370 °C, was ~150 even with thicknesses ≤15 nm. The recent development of novel group II precursors made it possible to increase the growth rate largely while leaving the electrical properties of the ALD $SrTiO_3$ film intact. This is an important advancement toward the commercial applications of these MIM capacitors to DRAM as well as to other fields, where an extremely high capacitor density and three-dimensional structures are necessary.

1. Introduction

The capacitor is an electric charge storing device that is used in a wide range of electric and electronic applications. Very large scale capacitors are being explored, even in energy storage devices for the most effective energy usage.[1,2] In microelectronic devices, capacitors serve mainly as for electric charge storage and noise reduction components. Among the many semiconductor-related microelectronic devices, dynamic random access memory (DRAM) is possibly the device that depends mostly on the performance (high capacitance density with extremely low leakage current and low loss factor) of the capacitors. This is because the presence or absence of charge (or voltage) in a cell capacitor (see **Figure 1a** for schematic diagram of DRAM cell), which is accessed through a select (or cell) transistor, represents the 1 or 0 digital data, respectively. The ever-shrinking dimensions of DRAM cells with the increasing packing density have made the cell transistor and capacitor size increasingly smaller. As the DRAM senses digital data by the detecting the change in voltage of a bit line ($\Delta V_b = \alpha V_{dd} C_c/(C_b + C_c)$, where V_{dd}, C_c, and C_b are the operation voltage, cell capacitance, and bit line capacitance, respectively, and α is a constant <~1/2) when the capacitor charge is dumped into it, a smaller sized capacitor requires higher capacitance density. The minimum ΔV (~100–150 mV) required has not been scaled as much due to the finite noise of the sense amplifier, and the capacitor burden of the scaled DRAM increases with decreasing V_{dd}. The degraded on/off switching performance of a cell transistor, which is quite detrimental to the writing into and keeping the data in the capacitor, has been alleviated by adopting a three-dimensional (3D) structure (e.g., recessed cell array transistor).[3] Therefore, the importance of the capacitor in DRAM is becoming more evident.

DRAM capacitors exist as trench and stacked types. However, as the trench type capacitors fade away from a ~50–60 nm technology node,[4] the only feasible way to obey Moore's law is to use a higher dielectric constant (ε) material in conjunction with the metal electrode in a capacitor. Figure 1b shows the evolution in the capacitor dielectric and electrode material along with the structures over the past decade

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and next years. It is apparent that an increasingly higher ε material has been used with the shrinking design rule. The major problem with a higher ε material is two-fold. It is usually accompanied with a decreasing energy gap (E_g),[5] which basically increases the risk of leakage-failure. The other is that a crystalline structure is needed to realize a higher ε. This usually does not favorably match with the extreme 3D structure of the DRAM capacitors because the optimal dielectric performance of a crystalline higher ε material is not necessarily guaranteed over a complicated 3D structure. There may be locally different compositions and crystalline structures depending on their location on the 3D structure. In addition, the generally rougher surface structure of a polycrystalline higher ε material also degrades the leakage current performance.[6]

There have been immense engineering efforts to optimize the capacitor structure using an appropriate combination of higher and lower ε materials, and a metal electrode. The most recent approach for this can be found from the tri-layered structure of tetragonal (or cubic) ZrO_2 ($\varepsilon \approx 40$)/amorphous Al_2O_3 ($\varepsilon \approx 9$)/tetragonal (or cubic) ZrO_2 with TiN electrodes (called ZAZ capacitor).[7,8] The use of TiN instead of conventional heavily doped poly-Si as an electrode also help improve DRAM capacitors owing to its higher electrical conductivity (negligible carrier depletion thickness) and absence of low ε interfacial SiO_2. It should be noted that TiN has a higher mechanical strength than poly-Si, which is another critical factor for fabricating extremely tall 3D capacitors. All these engineering efforts have ensured the success of DRAM, which does not appear to have been replaced by any other type of memory for use as the main memory of a computer in near future, down to ~45–50 nm technology node. In these DRAMs, a minimum equivalent oxide thickness (t_{ox}) of ~0.7–0.8 nm and a capacitor height of ~2 μm with a cylindrical structure is used. This has been well summarized by Kuesters et al.[9] In addition, Niinistö et al. summarized the recent trends of atomic layer deposition (ALD), which is obviously the process of choice for the dielectric and electrode for such an extreme geometry, of these higher ε materials including the newly-highlighted rutile-structured TiO_2.[10]

Along with these group IV binary oxides (and their slight modification by doping), there have been extensive studies of perovskite dielectrics, most typically $SrTiO_3$ (STO), which may offer a much larger ε value.[11] However, perovskite oxides have two serious disadvantages. First, their ε severely decreases with decreasing physical thickness in the range of interest. This has been dealt with extensively, both experimentally and theoretically.[11–14] The second is the much more complicated processes compared to binary oxides due to their multi-cation composition. The optimum ε value is acquired only in a very narrow stoichiometric range.[15–18] This has also been studied extensively in metal-organic chemical vapor deposition (MOCVD)[15,16] and ALD.[17,18] In addition, the TiN electrode appears to be incompatible with these very high ε materials due to (local) lattice mismatch, chemical interactions (interfacial oxidation and reaction), and low work function. This is also the case for the rutile TiO_2. Therefore, there is a strong need for better electrodes. Ru or RuO_2 appear to be the most promising material at this moment.[19,20]

This article summarizes the authors' recent research results in the field of higher ε dielectric films including TiO_2- and STO-based materials as well as Ru/RuO_2 electrodes aiming at

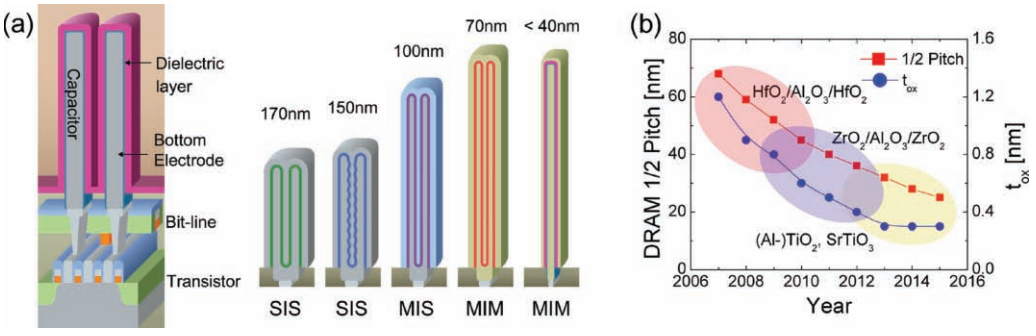

Figure 1. a) Schematic diagram of DRAM cells and a summary of the DRAM capacitor technologh evolution. b) Evolution in the capacitor dielectric and electrode material along with the structures over the past decade and next several years.

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t_{ox} < 0.5 nm. Such a challenging t_{ox} value will become necessary as the capacitor structure can no longer be cylindrical, as shown in Figure 1a, which will drastically decrease the surface area compared to previous generations. These topics have been dealt with by many other researchers but are not reviewed extensively in this article because they were recently summarized.[9,10] However, some of them are discussed in the necessary comparison with the authors' own results.

Before discussing the experimental results, the recent theoretical understanding on the dielectric properties of the metal/dielectric interface are discussed briefly because this may be closely related to the ultimate limit of decreasing the t_{ox} for any given metal/dielectric/metal capacitors. The importance of the interface increases for such extremely scaled DRAMs capacitors because the physical thickness of the dielectric and metal electrode should be <~10 nm (Figure 1a).

2. Results and Discussion

2.1. The Metal/Dielectric Interface from the Theoretical Point of View

The metal/high-ε dielectric interface usually suffers from degraded dielectric properties for various physical, chemical and electrostatic reasons.[13,14,21,22] In practice, complete elimination of interfacial contamination is almost impossible, even under the highly controlled environment of the DRAM fabrication lines. High-ε materials are usually chosen based on their bulk dielectric constant, which implicitly assumes that the dielectric constants are well maintained in the thin film structures. For many dielectric materials, this premise appears to be valid down to the nanometer scale.[23,24] However, ferroelectric materials that possess large ε vales (≥100) challenge this assumption. In particular, the dependence of the dielectric constant on the thickness indicates the presence of an interfacial layer with a significantly lower dielectric constant than the value expected for the bulk. This layer is usually called the "dielectric dead layer," which suggests that the region is not functioning as the desired dielectric media. A dead layer was found even for epitaxial STO grown without thermal strain.[25] The existence of a dead layer will create a significant hurdle in future microelectronic devices. Therefore, considerable theoretical and experimental research effort has been devoted to understanding this phenomenon. The mechanism proposed to date can be divided into extrinsic and intrinsic effects. As extrinsic effects, the presence of dislocations, secondary phases and atomic inter-diffusion can distort the dielectric response at the interface. However, even if a metal-insulator interface is formed without imperfection and maintains the atomic sharpness, the interfacial dielectric constant can be different from the bulk. For example, it was suggested that field penetration into a metallic electrode can act as a dead layer.[13]

In the conventional first-principles method, the Fermi level should be uniquely defined throughout the whole system. However, this is not compatible with the capacitor structure under a finite bias because the Fermi levels in the two electrodes are different. This was resolved in two recent developments,[26,27] which enabled an investigation of the interfacial dielectric response on the atomic scale. In Ref.,[26] the use of localized Wannier functions allowed the polarization in the periodic metal-insulator heterostructures to be defined. A more straightforward approach was suggested in Ref.,[27] where the metal-insulator slab was used to describe half of the capacitor structure. The change in the electrostatic potential perturbed by the external bias provides information on the local dielectric response. Both methods should yield similar results as far as the surface effects in Ref.[27] can be ignored. Indeed, the results on Ag/MgO in Ref.[26] and Au/MgO in Ref.[27] agree well with each other. However, the local dielectric permittivity is more diffused within the Wannier-function approach, which overestimates the penetration depth of the metal electrodes. From the application to the ideal $SrRuO_3$/STO interface,[28] it was found that the dielectric constant of STO is reduced significantly near the interface. In particular, when the thickness of STO is 2.7 nm, the calculated capacitance is 258 fFμm^{-2}, which is much lower than the nominal value of 1600 fFμm^{-2}. In other words, the average dielectric constant is only ~80, which is one sixth of the theoretical bulk value (~490). The microscopic origin of the dead layer was attributed to the hardening of the lowest optical phonon mode, which accounts for most of the static dielectric constants. **Figure 2** shows the estimated t_{ox} versus the STO thickness deduced from the theoretical results on the $SrRuO_3$/STO/$SrRuO_3$ capacitor in Ref.[28]. The bulk dielectric constant was set to 490 (theoretical value) and 300 (experimental value) for the solid and dashed lines, respectively. Since t_{ox} for a 12 nm-thick STO is approximately 0.65 nm experimentally (vide infra), Figure 2 suggests that there may still be room for further improvement. The dielectric dead layer was also found for Ni/ZrO_2 interface.[27] One interesting observation in Ref.[27] is that the interfacial capacitance associated with the field penetration into the metal should be >1000 fFμm^{-2} for both Au and Ni electrodes. This value is much higher than the estimations based on the Thomas-Fermi approximation in Ref.,[13] which is ~200 fFμm^{-2} for pure metals, such as Pt or Cu. An inspection of the electrostatic potential showed that the uniform electric field is screened extremely well and the field penetration into the metallic layer (defined by the outermost atomic positions) is negligible. Therefore, the Thomas-Fermi method in Ref.[13]

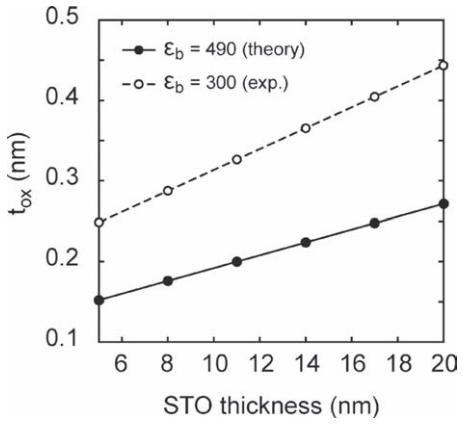

Figure 2. Predicted t_{ox} versus the thickness of STO inferred from the results in Ref.[28].

certainly underestimates the screening capability of a uniform metallic surface. However, the interface roughness in real situations can compromise the metallic screening and result in finite field penetration. In addition, the existence and severity of the dead layer may vary over different combinations of electrodes and dielectrics.[28,29] For example, it was found that the interfacial effect is not significant in Pt/HfO_2 and RuO_2/TiO_2 interfaces.[30] This suggests that the theoretical guideline would be useful for choosing the dielectric materials and metal electrodes to achieve the high density of capacitance.

2.2. TiO_2-Based Binary High ε Dielectric Films: Processing and Material Performances

2.2.1. Rutile TiO_2 Thin Film Growth by ALD

TiO_2 with a rutile structure is quite eccentric in terms of the dielectric constant among binary oxides. Its very high ε value (170 and 90 along the c- and a-axis of its tetragonal crystal structure)[31] is due to the very high Born effective charges of Ti and O ions and the soft optical phonon mode in the crystal structure.[32] Although this material has been overlooked in high-ε gate insulators of field effect transistors due mainly to the interfacial instability with the Si substrate,[33] the use of the metal electrode of the DRAM capacitor, particularly Ru and RuO_2, does not have such a problem.

There are many reports on the CVD and ALD of TiO_2 films on a variety of substrates owing to its viable features in various applications, all of which cannot be referred in this article. The films can be grown with amorphous[34,35] or crystalline structures (brookite,[36] anatase,[37,38] and rutile[39,40]) depending on the processing conditions (most importantly the growth temperature) and precursors. However, the stringent requirement of the very conformal deposition over the extreme 3D structure of a DRAM capacitor obviously prefers the film being grown by ALD. However, most Ti-precursors decompose thermally at temperatures (≥400 °C) where the desired rutile structure is achieved when a non-lattice matched substrate is used.[41,42] Anatase has a much lower dielectric constant (~35–40) and brookite is unstable. Halide precursors, such as $TiCl_4$ or TiI_4, can withstand high temperatures[39,43] but these precursors are much less compatible with the mass-production worthy ALD tools.

It was also reported, however, that the epitaxial growth of a TiO_2 film is possible even at a temperatures as low as 400 °C on a lattice matched substrate without requiring a high-vacuum environment.[44] This suggests that the crystalline structure of the TiO_2 can be easily controlled with respect to the type of substrate. According to this idea, the authors reported a rutile structured TiO_2 thin film growth on a Ru substrate at temperatures as low as 250 °C,[45] at which most of the MO-precursors remained intact, enabling a fluent ALD reaction to occur. The important factor was forming the interfacial RuO_2, which has also a rutile structure and a good lattice match with rutile TiO_2. RuO_2 can be grown either by in-situ or ex-situ methods.[45–47]

The most commonly used MO precursors for Ti are alkoxides, most typically Ti-tetra-isopropoxide (TTIP), which has a high enough vapor pressure (100 mTorr at 30 °C) and a reasonably high thermal decomposition temperature (~280 °C) in typical ALD reactors. ALD TiO_2 films were grown on Si, Pt and Ru substrates at temperatures ranging from 200 to 280 °C using H_2O or O_3 as the oxygen source.[45,48] When the films were grown on non-lattice matched substrates (Si and Pt) amorphous (near 200 °C) or anatase (~225–280 °C) TiO_2 films were grown, irrespective of the oxygen source.[45,48] The crystallization and growth rate was also dependent on the film thickness on the Si substrate. When the films were quite thin (<~10 nm at 250 °C), amorphous films were grown with a lower growth rate (0.038 nm/cycle) but they crystallized with a sudden increase in roughness and growth rate (0.2 nm per cycle) over that thickness.[48] Using O_3 as the oxidant, this transient behavior was not observed with a constant saturation growth rate of ~0.05 nm per cycle.[45] However, all these films are not promising as a DRAM capacitor dielectric due to their lower ε value (35–40) with relatively high leakage current.[45,48]

Rutile TiO_2 thin films were grown on a Ru electrode when the Ru surface was oxidized to RuO_2 either by the strong oxidation potential of the O_3, O_2-, or N_2O-plasma oxygen sources at a growth temperature of 250 °C.[45,49,50] The rutile crystal structure of TiO_2 films was identified by X-ray diffraction and electron diffraction. More importantly, the bulk ε value extracted from the inverse slope of graph of t_{ox} vs. physical thickness (t_{phy}) (**Figure 3a**),

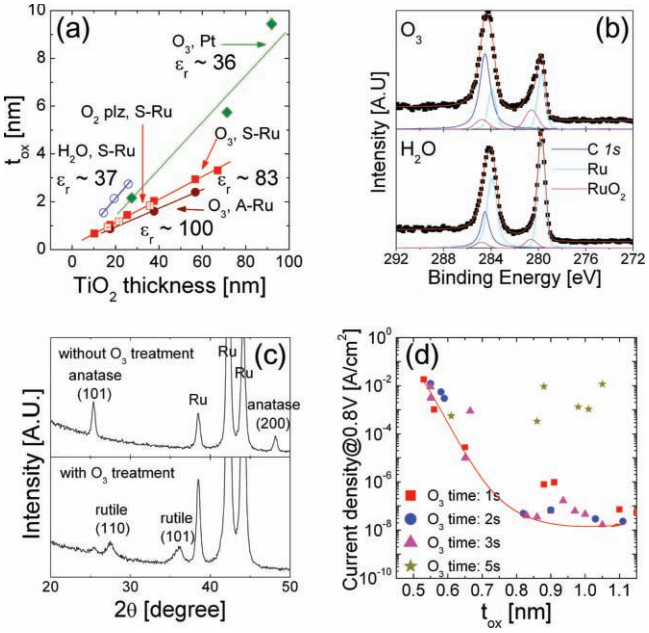

Figure 3. a) Variation in the t_{ox} of TiO_2 films grown on various substrates as a function of film thickness.[45,56] (A-Ru: ALD Ru, S-Ru: sputtered Ru, two Ru substrates have different preferred orientation.) Reproduced with permission.[45] Copyright 2004, American Institute of Physics. b) Ru 3*d* XPS spectra of Ru substrates below 1 nm thick TiO_2 films, which are grown using O_3 and H_2O as the oxygen source, respectively.[45] Reproduced with permission.[45] Copyright 2004, American Institute of Physics. c) GAXRD spectra of TiO_2 thin films on a Ru substrate with and without O_3 pretreatment.[46] Reproduced with permission.[46] Copyright 2006, American Institute of Physics. d) Relationship between t_{ox} and current density of TiO_2 films at an applied voltage of 0.8 V with various O_3 feeding times.[53] Reproduced with permission.[53] Copyright 2007, American Institute of Physics.

which represents more accurately the crystalline phase and preferred orientation free of the possible interface effect, was as high as 80–100.[45] Figure 3b shows the X-ray photoelectron spectra (XPS) of the Ru 3*d* peak from Ru substrates under 1 nm-thick TiO_2 films grown using O_3 (concentration ~ 400 Ng/m^3) and H_2O as the oxygen source, respectively.[45] A clear and stronger XPS signal from the RuO_2 phase was detected from the sample with O_3 reaction gas. H_2O appears to oxidize Ru slightly but its coverage over the Ru surface was not sufficient to induce rutile TiO_2 growth.

It was later found that with the appropriate pre-oxidation of the Ru surface in an O_3 atmosphere (concentration ~400 Ng m^{-3}) at ~250 °C, prior to TiO_2 deposition, ALD with the less oxidizing H_2O oxygen source would still induce rutile TiO_2 film growth at the same growth temperature.[46] Figure 3c shows the XRD pattern of 27 nm-thick TiO_2 films on the non- and O_3-pre-treated Ru substrates, respectively, when the TiO_2 film was grown with H_2O. It is obviously identified that rutile TiO_2 was grown on the O_3-pre-treated Ru substrate. Similar results were reported by other groups, not only on the RuO_2 but also on IrO_2.[47,51,52] They commonly reported that local-epitaxy induced rutile TiO_2 growth at temperatures <~300 °C.[51,52]

The generation of denser and smooth RuO_2 on the Ru surface is the governing factor for achieving phase-pure and low-leakage TiO_2 films. The degree of Ru surface oxidation during the ALD of TiO_2 was controlled by varying the O_3 pulse time during ALD, and the resulting electrical performance was examined (Figure 3d).[53] Up to a O_3 pulse time of 3 s, all the leakage vs. t_{ox} data aligned on a single line suggesting that Ru had been appropriately oxidized with only a 1 s O_3 pulse time. However, when the O_3 pulse time was increased to 5 s, the leakage current was increased significantly due mainly to the increased roughness of the substrate. The root-mean-roughness measured by atomic force microscopy of the film for the O_3 pulse time of <3 s and 5 s was ~1 and ~3 nm, respectively.[53] The surface roughness is a critical factor that affects the leakage current, as discussed in section 2.4.

Although these are quite promising results, there are two concerns regarding rutile TiO_2 films. The first is that the ε value of the rutile TiO_2 film was not as high as the bulk value along the c-axis. This might be due to the less optimum crystallographic growth direction of the film. In Figure 3a the two different ε values (83 and 100) were achieved from TiO_2 films on the sputtered and ALD Ru electrodes, respectively, where the two Ru films have different preferred growth directions.[45] The second was that the leakage current was rather high due to the relatively small E_g (~3.1 eV) and the n-type nature of TiO_2 that forms the Schottky barrier height for electron transport with a magnitude ~1 eV either with Pt and RuO_2 electrodes.[54] These two problems are dealt with in the following sub-sections.

In passing, it was noted that a certain growth rate (roughly 0.05 nm min^{-1}) of TiO_2 films was necessary to suppress the desorption of RuO_2. When this growth rate was not reached, the Ru substrate was actually etched away through a disproportionation reaction ($2RuO_2 \rightarrow Ru + RuO_4$).[55] This severely interferes with any oxide film growth on a Ru electrode using O_3 as the oxygen source.

2.2.2. Rutile TiO_2 Film on Ru/TiN Electrode

Although Ru offers a feasible route for growing rutile TiO_2 films in a reasonable ALD window, a single layered Ru bottom electrode structure may not be commercially used in DRAM due to its high cost. A much more plausible method is to deposit a thin (<<5 nm) Ru film on the TiN bottom electrode structure, of which the fabrication process is well matured. Therefore, the bottom electrode structure is most likely double-layered (Ru/TiN) or even triple-layered (RuO_2/Ru/TiN), as shown in Figure 1a. Interestingly, the preferred growth direction (101 direction) of Ru films by ALD on a TiN electrode, which is discussed more in section 2.4, is different from the crystallographic orientation of the sputtered films (more or less random or 002 direction preferred).[56] The rutile TiO_2 film on the optimized Ru (~2–3 nm-thick)/TiN electrode showed a ε value as high as 133.[56] Therefore, there may be more room for further improving the ε value toward 170, which is the value of a single crystal along the c-axis if the TiO_2 film the growth direction approaches the c-axis.

The growth of a Ru layer on a TiN electrode either by ALD or CVD is somewhat difficult due to the delayed nucleation of the Ru layer on the TiN.[57,58] This delayed nucleation of Ru was improved considerably when the TiN surface was activated by an Ar-plasma treatment[56,58] immediately before TiO_2 ALD. **Figure 4a** shows a cross-section transmission electron microscopy (TEM) image of TiO_2/thin Ru (~5 nm)/TiN electrode that was grown on a poly-Si layer. The growth behavior of the Ru layer was quite different from the ideal case, which shows a uniform and smooth growth. Due to this abnormal behavior,

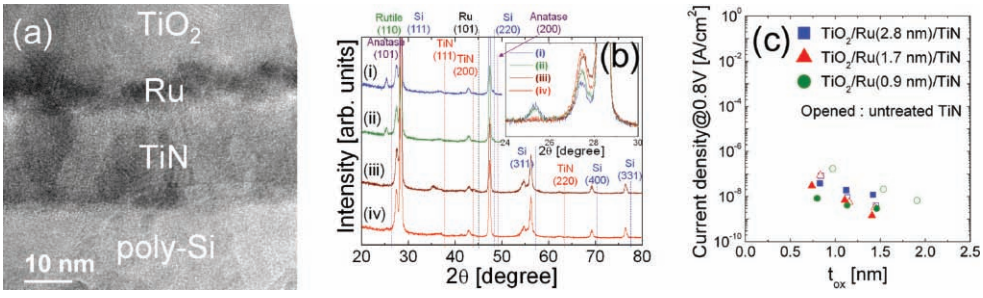

Figure 4. a) Cross-section TEM image of TiO_2/thin Ru/TiN/poly-Si stack structure. b) GAXRD patterns of 40 nm-thick TiO_2 on i) (100 cycle)/untreated TiN, ii) Ru(100 cycle)/Ar plasma-treated TiN, iii) Ru (200 cycle)/untreated TiN, and iv) Ru (200 cycle)/Ar plasma-treated TiN. c) Overall dielectric performance of TiO_2/thin Ru/TiN stack structures.[56] Reproduced with permission.[56] Copyright 2009, American Institute of Physics.

there were several spots where the TiN was not coated with Ru when it was not thick enough (≥ ~5 nm). These spots eventually resulted in the formation of anatase TiO_2 because TiO_2 grows in that form on TiN. Figure 4b shows the grazing angle incidence XRD (GAXRD) patterns of the 40 nm-thick TiO_2 films grown by a plasma-enhanced ALD at 250 °C on the Ru/TiN stacked electrode layers.[56] Here, the TiN electrode was either Ar-plasma treated or untreated prior to Ru ALD, and Ru ALD cycles of 100 and 200, respectively, were adopted. When the Ru layer was thick enough (200 cycles), almost phase-pure rutile TiO_2 was formed, whereas a thinner Ru layer (100 cycles) on the non-treated TiN resulted in mixed rutile-anatase TiO_2 films. The TiO_2 film on the thinner Ru/plasma-treated TiN showed a negligible contribution from the anatase phase. The overall dielectric performance was also affected by the single phase formation, as shown in Figure 4c. The decreased ε value of the TiO_2 films on thinner Ru (<~2 nm)/non-treated TiN resulted in higher t_{ox} values at a given leakage current.[56]

2.2.3. Al-Doped TiO_2 Film for Abrupt Decrease of the Leakage Current

The results shown in sections 2.2.1 and 2.2.2 show that rutile TiO_2 is a promising capacitor dielectric in future DRAMs owing to its high ε value compared to other binary oxides, such as HfO_2 and ZrO_2. However, its lower E_g and n-type nature generally results in a relatively high leakage current density, which limits the minimum achievable t_{ox} value to ~0.8 nm satisfying the leakage current density specification ($<1 \times 10^{-7}$ A cm^{-2} at an expected capacitor voltage of ~0.8 V). Indeed, the relatively small E_g itself is not a direct source of the large leakage current. Leakage current mechanism analysis of Pt/TiO_2/(RuO_2)Ru structure showed that leakage current flow was governed by the Schottky emission at the metal/dielectric interface, suggesting that the interfacial Schottky barrier height (ϕ_b) is the factor governing leakage current.[54] If the Fermi level of an electrode is located at the center of the E_g, both the electron and hole barrier heights are ~1.5 eV, which is large enough to sufficiently suppress carrier injection. However, the estimated ϕ_b for electron injection was only ~1 eV, suggesting that the Fermi level was pinned to the upper half of the E_g of TiO_2. This is probably due to the surface charge screening effect by the donor state formed inside TiO_2. TiO_2 is a well-known n-type wide band gap material due to electron self-doping by oxygen vacancies (V_O).[59] Therefore, it was expected that acceptor doping (in this case Al) can compensate for the donor state and move the pinned Fermi level to a more optimal position. In addition, Al doping by ALD is a feasible method because of the very well established Al_2O_3 ALD process.[60,61] Actually, the role of Al in TiO_2 is more complicated than such a simple acceptor doping model suggests, as revealed in detail in Ref.[54].

Doping with Al was accomplished by replacing one of the TiO_2 deposition cycles (60–120) with an Al_2O_3 cycle. **Figure 5a** shows the schematic energy band structure at the Pt/TiO_2 and Pt/ATO (ATO stands for the Al-doped TiO_2) interfaces estimated by an analysis of the leakage current and XPS.[54] A first-principles calculation showed that the large E_g (~8 eV) of Al_2O_3 does not increase the E_g of the ATO film. This is due to the limited hybridization of Al2*p* and Ti3*d* orbitals that constitute

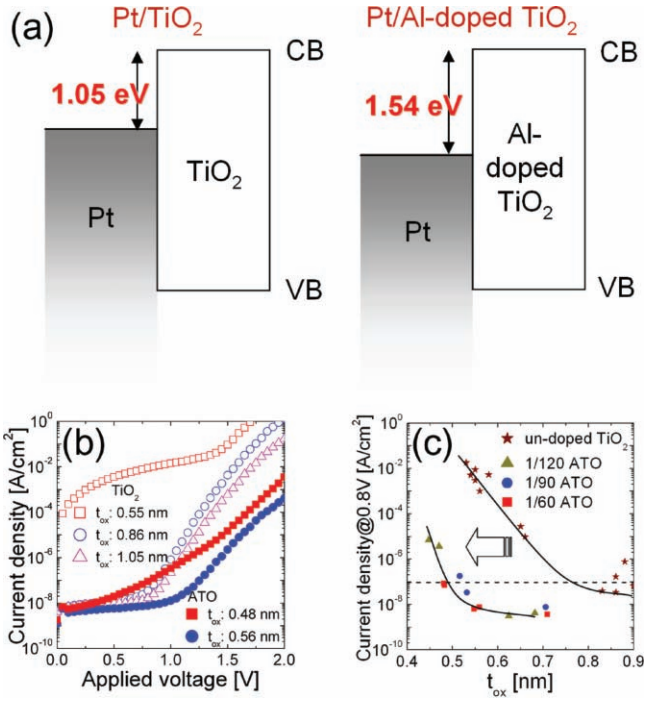

Figure 5. a) Schematic energy band structure at the Pt/TiO_2 and Pt/ATO interfaces. b) *J–V* curves of TiO_2 and ATO films on Ru electrodes. c) Overall summary of leakage current density at 0.8 V vs. t_{ox} for TiO_2 and ATO thin films.[54] (1/60, 1/90, and 1/120 stand for the Al/[Al±Ti] precursor feeding cycle ratio.) Reproduced with permission.[54] Copyright 2008, Wiley-VCH.

the conduction band. Therefore, the increased ϕ_b (~1.5 eV) for electron injection for the Pt/ATO interface was attributed mainly to electro-static interactions between the interface Al ions and metal electrode, which induced suitable charge transfer.[54] Due to this optimized energy band shape near the interface, the leakage current density was decreased by ~10^6 times at the $t_{ox} \approx$ 0.5–0.6 nm. (Figure 5c). Figure 5b shows the typical current density–voltage (*J–V*) curves of the TiO_2 and ATO films showing the largely suppressed *J* of the TiO_2 film by Al-doping.

Another interesting aspect is that there is a certain optimum Al concentration (~20 at%) at the metal/ATO interface (especially for RuO_2/TiO_2), where the system energy is minimized.[54,62] Along with the very rapid diffusion rate of Al in a growing TiO_2 film at 250 °C along the thickness direction, this thermodynamic driving force results in an almost identical interfacial Al concentration irrespective of the bulk Al-doping concentration.[62] It should be noted that the interfacial Al concentration is the key factor in reducing the leakage current density.[54] Therefore, this is a very promising property of the system, which can withstand the process variations. Further improvements in ATO on a RuO_2 electrode is reported in section 2.4.

2.3. $SrTiO_3$ Dielectric Thin Films: Precursor, ALD Process, and Performances

STO must obviously be a better capacitor dielectric than TiO_2 or ATO in terms of the ultimately achievable dielectric constant

at room temperature (~300) given similar E_g (~3.2 eV). However, this is not necessarily the case when the film becomes thin enough to be used (<~10 nm) in highly scaled DRAMs. This is due to the degraded dielectric performance of the metal (or conducting oxides)/dielectric interface, as discussed in section 2.1. It has been reported extensively that achieving the promising dielectric performance of STO films with thicknesses <~20 nm is not trivial even by sputtering.[63–66] This becomes even more obvious when the technically DRAM-compatible MOCVD and more preferably ALD processes are considered.

Approximately 10–15 years ago, there was extensive research on MOCVD of STO and (Ba,Sr)TiO_3 thin films.[67–70] However, they were not successful enough to be adopted in DRAMs for several reasons; immature MO precursor technology particularly for Sr (and Ba too), difficulty in achieving thickness and composition step coverage on an extreme 3D geometry,[71,72] and insufficiently high growth rate. While sluggish improvement has been made in this field, the much faster development in simpler binary oxides, such as Al_2O_3, HfO_2, and ZrO_2, due to the rapid improvements in ALD techniques has become the mainstream of DRAM capacitor technology. Currently, the necessity for STO is returning due to the need for an extremely small t_{ox}. Nevertheless, accumulated knowledge of the chemical reaction route of group II element precursors and realizing the complexity in fabricating 3D structures by MOCVD[73,74] has greatly assisted in the development of an ALD process of STO.[17,18,75–81]

ALD of multi-cation perovskite oxides (ABO_3) is quite interesting in many aspects. Ideally, the alternating growth of AO and BO_2 with their fully saturated surface coverage would result in an invariant A/B ratio in the film, which is totally determined by the chemistry used. However, steric hindrance from volumetric precursor molecules usually results in partial coverage of the surface in a single growth cycle. Thus, the appropriate selection of cycle ratio (m/n, where m and n are the cycle numbers of AO and BO_2, respectively, or SrO and TiO_2 in this case) has produced precise composition control to a stoichiometric Sr/Ti ratio in the film.

In the early stages of ALD STO research, the most common Sr-precursor was $Sr(tmhd)_2$ ($Sr(C_{11}H_{19}O_2)_2$), (tmhd = 2,2,6,6-tetramethyl-3,5-heptanedione), which was reported to have limited ALD reactivity with H_2O,[79] even though ALD of SrS using the same precursor has been reported to be feasible.[82] Therefore, an oxygen source with higher reactivity, such as O_3, has been used to induce a more active ALD reaction with the $Sr(tmhd)_2$ precursor.[80] However, $SrCO_3$ films were grown instead of SrO, which was not alleviated even by combining TiO_2 layer growth. Ahn et al. used O_2-plasma for the same Sr-precursor, and achieved almost carbonate-free STO films in ALD mode as well as promising electrical properties of the films after the appropriate post-deposition annealing (PDA) to crystallize them. However, they did not report the step coverage.[81] There is some concern with plasma-based ALD processes in terms of the step coverage over a severe 3D geometry. There was an earlier report of the ALD of STO and $BaTiO_3$ films using the modified cyclopentadienyl (Cp)-based group II precursors and H_2O as the oxygen source.[75] These precursors react with H_2O but their limited thermal stability during vaporization and thermal decomposition behavior at the typical ALD temperature window (< ~350 °C) has hindered the further improvement of this process.[79]

The authors revisited an earlier report of the ALD and MOCVD of STO films,[70,83] and found that the $Sr(tmhd)_2$ precursor was usually vaporized at temperatures higher than its melting temperature (~200 °C) to achieve a high enough vapor pressure. However, this was also a viable condition for the oligomerization of the precursor molecules of which the chemical reactivity with H_2O should be degraded significantly compared to that of the monomer molecules.[76] Therefore, the vaporization of $Sr(tmhd)_2$ precursor at temperatures <200 °C (typically 180–190 °C to achieve a not too low vapor pressure) was adopted and the more monomer-like $Sr(tmhd)_2$ precursor molecules were vaporized. They react with H_2O to form SrO (not $SrCO_3$) and STO films when combined with the TiO_2 ALD steps at a typical growth temperature of 250 °C.[76] The self-limiting growth behavior with respect to the precursor pulse, oxygen source pulse and purge time was confirmed showing that a genuine thermal ALD reaction can be achieved using this method.[76,77] **Figure 6** (a) shows the changes in the growth rate of SrO and STO films as a function of the vaporization temperature of $Sr(tmhd)_2$. The graph shows the fluent ALD growth of SrO and STO when the monomer-like $Sr(tmhd)_2$ molecules were supplied.[77] In addition, the growth rate of SrO was largely increased when it was intermixed with TiO_2 to grow STO films with respect to single SrO growth, which can be ascribed to the catalytic effect of the TiO_2 surface. A highly conformal thickness and cation-composition step coverage over an extreme 3D geometry was also confirmed (Figure 6b).[76] However, the as-grown films were mostly amorphous with a fairly lower density than the theoretical value, which caused a serious problem during crystallization annealing. Here, the substrate was a typically sputtered Ru film. PDA at temperatures >~600 °C was performed to achieve the crystallized films but this also results in significant thickness shrinkage (~70%–80% of the original thickness, Figure 6c)[84] as well as micro-cracking along the grain boundaries. (Figure 6d)[77] This evidently degraded the leakage current density so that the crystallized films became incompatible with the DRAM application. These discouraging properties were attributed mainly to the low ALD temperature (<~280 °C), which resulted in an amorphous film, due to the limited thermal stability of Ti-precursor used, TTIP.

In an attempt to solve this problem, $Ti(O\text{-}iPr)_2(tmhd)_2$ ($Ti(O\text{-}i\text{-}C_3H_7)_2(C_{11}H_{19}O_2)_2$, abbreviated as Ti22 here) was used as the Ti-precursor, which showed a thermal decomposition behavior at ALD temperatures >~390 °C.[84] Even better thermal stability was achieved from the $Ti(t\text{-}BuO)_2(tmhd)_2$ but the extreme bulkiness of this Ti-precursor resulted in a non-stoichiometric film (maximum Ti concentration of ~ 20% was obtained in the film even at a very low Sr/Ti cycle ratio). Ti22 could achieve a Sr/Ti ratio of 50/50 in the film at an appropriate Sr/Ti cycle ratio. Therefore, the thermal ALD of a STO film was attempted using $Sr(tmhd)_2$ and Ti22 with H_2O at growth temperatures up to 390 °C (typically at 370 °C). The film density increased significantly with no notable thickness shrinkage after PDA (Figure 6c). The saturated ALD growth behavior with respect to the $Sr(tmhd)_2$ and Ti22 pulse time was also confirmed (**Figure 7a**).[84] However, the as-grown film was still amorphous on the

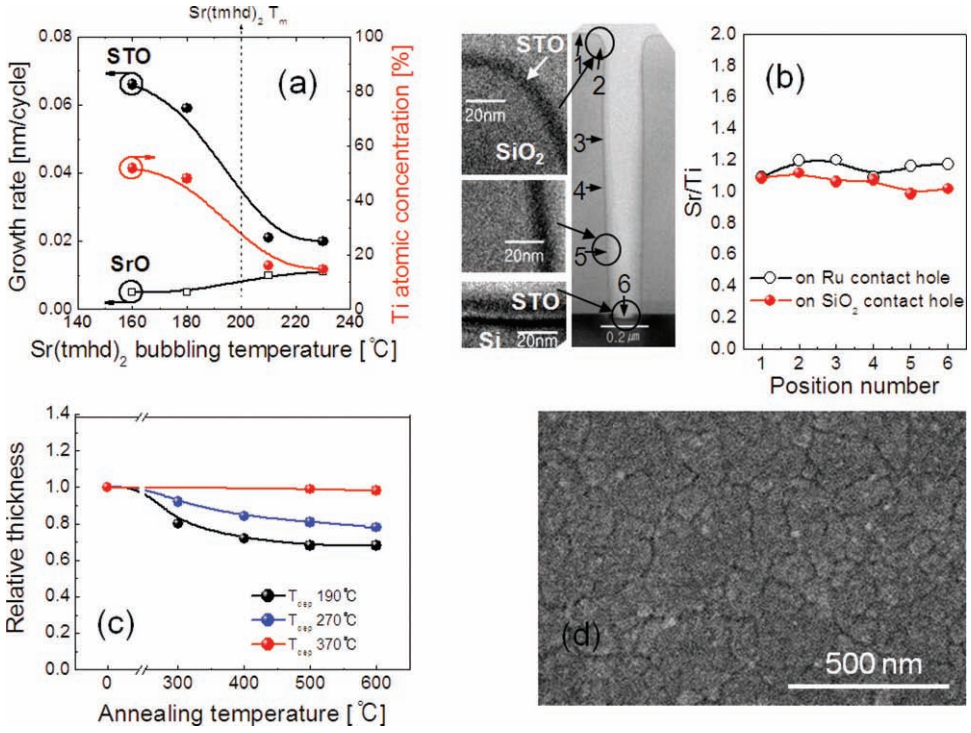

Figure 6. a) Variation in the growth rate of SrO and STO films as a function of vaporization temperature of $Sr(tmhd)_2$ which shows the fluent ALD growth of SrO and STO when the monomer-like $Sr(tmhd)_2$ molecules were supplied.[77] Reproduced with permission [77]. Copyright 2007, American Institute of Physics. b) Highly conformal thickness and cation-composition step coverage over an extreme 3D geometry.[76] Reproduced with permission [76]. Copyright 2005, American Institute of Physics. c) Thickness shrinkage depending on the PDA temperature.[84] Reproduced with permission [84]. Copyright 2008, American Institute of Physics. d) The creation of micro-cracking along the grain boundaries after the PDA.[77] Reproduced with permission [77]. Copyright 2007, American Institute of Physics.

non-lattice matched Ru electrode, and the PDA resulted in a large grain size (>>100 nm in diameter). There was little evidence that the Ru surface had been oxidized to RuO_2. The leakage current was not promising either after PDA, probably due to the presence of micro- or nano-scale cracks and crystallization-induced stress, even though the amorphous films were highly insulating (Figure 7b). Therefore, it became evident that the in-situ crystallization was inevitable to achieve a low enough leakage current. This was already reported for sputtered STO films even on a better lattice matched Pt electrode.[68] Moreover, a substrate temperature of at least ~450 °C was necessary to achieve in situ crystallization in the sputtering process.[68]

In situ crystallization in ALD was attempted using a so called two-step process, where the thin crystallized (~3–5 nm) layer of STO was deposited first followed by the main layer (>~10 nm) of STO.[84,85] The thin crystallized layer of STO (called the seed layer) can be grown by ALD at 370 °C, in which the film is still amorphous, followed by crystallization annealing at 650–700 °C. Due to local lattice match between the crystallized seed layer and main layer, the overall film was crystallized in situ with an average grain size of <<~50 nm (Figure 7c, where no boundary between the seed layer and main layer was observed). The in situ crystallized STO film was grown preferably along (100) orientation on Ru, confirmed by XRD examination. The crystallized seed layer appeared to contain a certain amount of $SrRuO_3$, which did not harm the in-situ crystallization process. The in situ crystallized film maintained a similar structure to the as-deposited film, resulting in very promising electrical properties (Figure 7d).

The structural and electrical properties of the STO film achieved by a two-step process appeared to be quite promising. However, the slow growth rate of the STO films (typically ~0.015 nm per cycle of each component cycle) was not compatible with the mass-production process.[84,85] In addition, the two-step process itself also takes a long time to complete the capacitor fabrication. This was attributed mainly to the slow growth rate of the SrO layer, which actually decreased the TiO_2 growth rate on top, even with the assistance of the catalytic enhancement of a TiO_2 layer. The TiO_2 growth rate using the Ti22 and H_2O was also quite slow (0.025 nm per cycle at 370 °C). This might be due to either a higher bonding energy between the β-diketone ligand with the Ti ions or the bulkiness of the precursors.

Holme and Prinz reported first and second ligand dissociation energies of various Sr- and Ba-MO precursor molecules based on the first-principles calculation results.[86] According to the report, Cp based ligands generally have a much lower first dissociation energy (~2.5–3.1 eV depending on the modified Cp ligand structure) than that of tmhd ligands (~5 eV). This can explain the insufficient thermal stability of the Sr- and Ba-precursors with the buthoxy-Cp ligands at these vaporization and ALD temperatures.[79] However, this problem was largely mitigated by better control of precursor-molecule synthesis process and higher purity. Moreover, the authors recently achieved a highly stable ALD process for STO films with

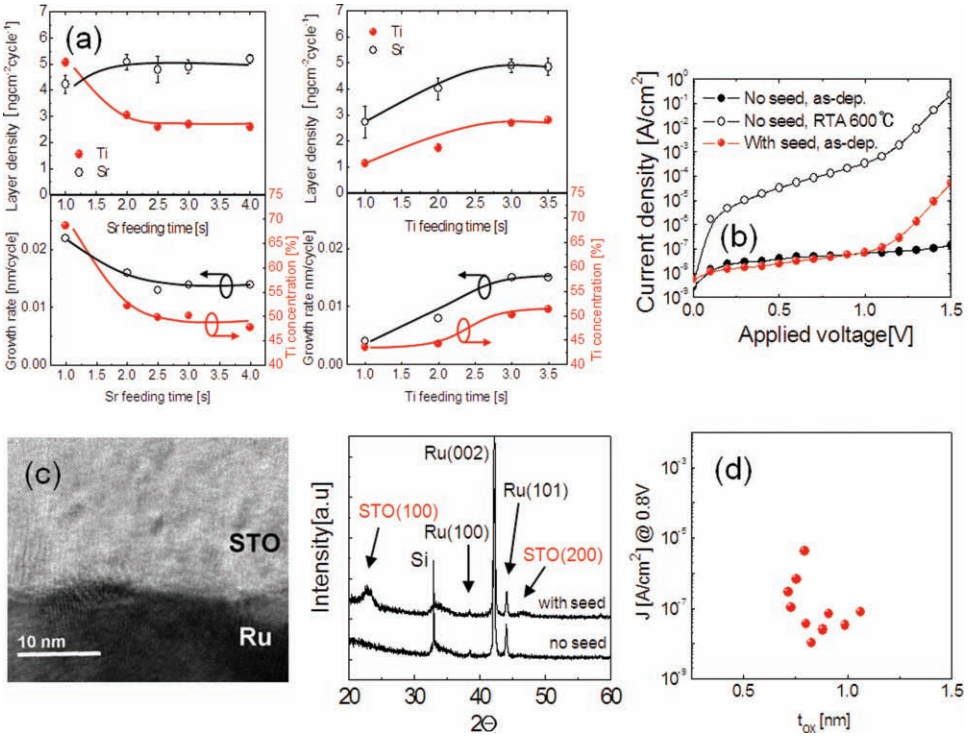

Figure 7. a) Saturated ALD growth behavior with respect to the (left) $Sr(tmhd)_2$ and (right) Ti22 pulse time at the growth temperature of 370 °C.[84] Reproduced with permission [84]. Copyright 2008, American Institute of Physics. b) Leakage current behavior of STO films when the seed layer was used or not. c) (left) TEM image of the in situ crystallized STO film with an average grain size of << ~50 nm, where no boundary between the seed layer and mainly was observed, (right) (100) preferred growth of STO film.[84] d) J (at 0.8 V) vs. t_{ox} performance showing very promising electrical properties of STO films. Reproduced with permission [84]. Copyright 2008, American Institute of Physics.

$Sr(iPr_3Cp)_2$ and Ti22, as shown below. The combined use of O_3 and H_2O as the oxygen source was essential for achieving a higher ALD temperature. In this study, O_3 and H_2O were used as the oxygen source for the growth of TiO_2 and SrO layers, respectively. H_2O was the preferred oxygen source considering the possible carbon contamination when O_3 was used. However, the $Sr(iPr_3Cp)_2$ precursor was prone to thermal decomposition at temperatures as low as 320 °C when they were pulsed on the OH-terminated surface. **Figure 8a** shows the change in the layer density of Sr as a function of the ALD temperature when the number of growth cycles was 33. Here, O_3 (abbreviated as SO process) or H_2O (abbreviated as SH process) was used as the oxygen source. The Sr layer density was generally higher when H_2O was used, indicating a stronger ALD reaction between the surface OH-group and this Sr-precursor. The Sr layer density increased abruptly at ~330 °C when H_2O was used, suggesting that thermal decomposition of the $Sr(iPr_3Cp)_2$ precursor began at this temperature. This agrees with previous reports.[79] However, this decomposition behavior can be retarded at higher temperatures (~390 °C) when O_3 is used as the oxidant (Figure 8a) or the Sr-precursor is pulsed onto the O_3-pulsed Ti-O surface, as shown in Figure 8b. Here, TH and TO correspond to the TiO_2 layer growth steps using H_2O and O_3, respectively, and each step was repeated twice before commencing a SH step. Interestingly, in the THSH process, the Sr-layer density increased abruptly at ~350 °C, suggesting that the Sr-precursor had decomposed thermally at this temperature, while it did not show such an abrupt change up to 390 °C in the case of the TOSH process. This suggests that the thermal decomposition of the $Sr(iPr_3Cp)_2$ precursor can be retarded in the ALD process of a STO film using O_3 as the oxygen source for Ti-precursor. More details on this ALD-STO process will be reported elsewhere.[87]

Therefore, STO film growth was achieved in ALD mode at a growth temperature of 370 °C with the TOSH process sequence due to the suppressed thermal decomposition of the $Sr(iPr_3Cp)_2$ precursor. Interestingly, Kosola et al. used the THSO process sequence to grow STO films using the $Sr(tmhd)_2$ and $Ti(OCH_3)_4$ as the Sr- and Ti-precursors, respectively.[80] With this process sequence, they encountered severe $SrCO_3$ formation.[80] Figure 8c shows the changes in the STO film thickness as a function of the unit cycle number on 3 nm-thick TiO_2 coated Ru (closed symbol) and bare Ru (open symbol) substrates when the TO : SH cycle ratio was 3:1 and 5:1, respectively. Here, the unit cycle number denotes the total number of TiO_2 and SrO cycles. (e.g., the total number of cycle was 100 when (3 TiO_2 cycles + 1 SrO cycle) was repeated 25 times) The growth rates calculated from the slopes were 0.107 and 0.075 nm per cycle when the TO/SH cycle ratio was 3:1 and 5:1, respectively. The larger growth rate for the 3:1 cycle ratio was due to the higher growth rate of the SrO layer than the TiO_2 layer.[87] These growth rates were 7 and 5 times faster than those of the ALD STO process using $Sr(tmhd)_2$ and Ti22, respectively. This is a very encouraging result in terms of mass-production compatibility.

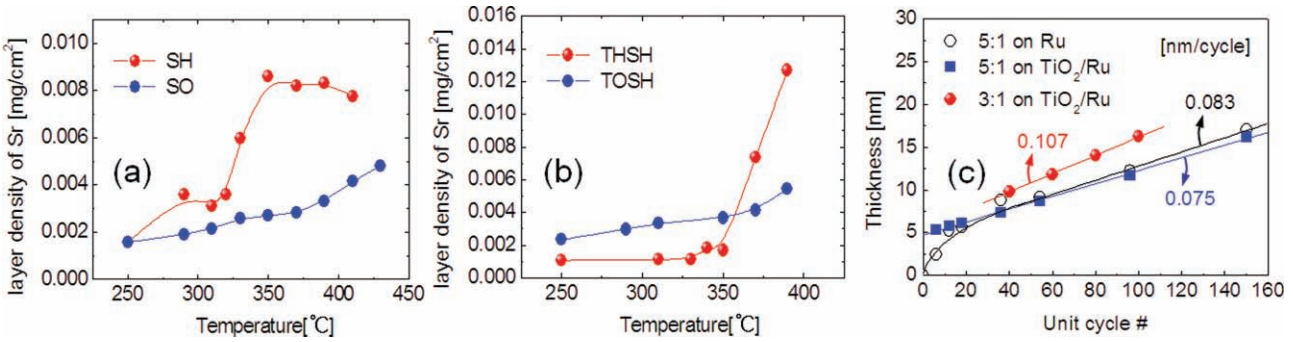

Figure 8. a) Growth characteristics of SrO with the sequences SH and SO as a function of the growth temperature on Ru substrate. b) Growth characteristics of STO with the sequences THSH and TOSH as a function of the growth temperature on Ru substrate. c) Growth rate of STO on Ru and TiO_2-coated Ru substrates at 370 °C with the sequence TOSH.[87]

The as-deposited film was also amorphous when no-seed layer was used. In addition, the incorporation of Sr onto the Ru surface was enhanced strongly compared to the TiO_2 layer, resulting in a Sr-rich composition at the film/Ru interface.[87] This prevented precise composition control to the stoichiometric Sr/Ti ratio and achieving promising electrical properties. Therefore, the Ru surface was coated with a ~ 3 nm thick TiO_2 layer before STO seed layer (4 nm thick) growth, which can suppress the enhanced Sr-incorporation. The thin STO seed layer was annealed as before and the main in situ crystallized STO layer was subsequently deposited. **Figure 9a** shows the change in the measured ε value of an 18~22 nm thick STO layer as a function of the Ti/Sr cycle ratio. The ε value showed a maximum value of ~90 at a Ti/Sr cycle ratio of 3:1, where the overall Sr/Ti ratio (51:49) of the film was closest to the stoichiometric value. This rather smaller ε value was attributed to the interface layer effect. Therefore, the bulk ε value was estimated from the inverse-slope of the t_{ox} vs. t_{phys} graph (inset figure of Figure 9a), and it was 146 suggesting a high quality STO layer despite its higher growth rate. Figure 9b shows a typical J–V curve of a 12.2 nm thick film (t_{ox} = 0.68 nm). The J value was maintained as low as ~2×10^{-8} A cm^{-2} at V ranging from −1.0 to 1.2 V. The inset figure in Figure 9b shows the J (at 0.8 V) vs. t_{ox} performance of the STO films. t_{ox} can be scaled down to <0.6 nm with a safe leakage current density. This is a very promising result considering the much higher growth rate. There may be room for further improvement by optimizing the bottom electrode, as shown in section 2.4.

The ALD of a STO film directly on a TiN electrode will eventually be necessary at the mass-production stage. Therefore, recent reports by the IMEC group are quite interesting and promising. They reported the ALD growth of a STO film using the $Sr(t\text{-}Bu_3Cp)_2$, $Ti(OCH_3)_4$, as the Sr- and Ti-precursors, respectively, and H_2O as the oxygen source at an ALD temperature of 250 °C.[17,88] The Sr-rich composition, which is generally less favorable than the stoichiometric composition on noble metal electrodes, was essential to achieve the optimal electrical properties (t_{ox} = 0.49 nm and J = ~10^{-7} A cm^{-2} at 0.8 V) when the maximum thermal budget was limited to 550 °C.[89] The bulk dielectric constant after crystallization annealing (the as-deposited film was amorphous) was ~150, which is similar to the present result. The authors' preliminary attempt to grow the STO films using this method was unsuccessful, probably due to the higher growth temperature (370 °C), which may induce severe oxidation of the TiN bottom layer. Further efforts in this area will be necessary.

2.4. Ru and RuO_2 Electrodes: Nucleation and Roughness

The considerable interest in the Ru layer as the metal electrode for MIM capacitors in DRAM was initiated by its easy dry etching capability using an O_2-plasma based etching gas.[90,91] Formerly, Pt had attracted a great deal of attention owing to its chemical inertness, high work function, and better lattice match with perovskite oxide dielectrics and ferroelectrics. However, the extreme difficulty in etching has yielded its position to Ru. Although a thick noble metal layer is not supposed to be dry-etched directly to form a 3D node structure in the present integration scheme (Figure 1a), Ru has another merit over Pt. As shown in Figure 1 and discussed in detail in section 2.2.2, the most feasible storage node structure will be a Ru/TiN double or RuO_2/Ru/TiN triple layer. RuO_2 may form a more favorable interface with the dielectric layer, as discussed in section 2.1.

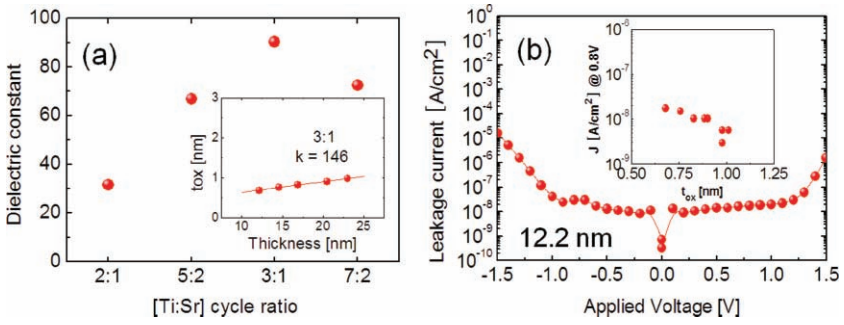

Figure 9. a) Variation of the measured ε value of the 18~22 nm thick STO layer as a function of Ti/Sr cycle ratio. inset) The bulk ε value estimated from the inverse-slope of the t_{ox} vs. t_{phys} graph at a cycle ratio 3:1. b) A typical J–V curve of a 12.2 nm thick film (t_{ox} = 0.68 nm) which shows very low leakage current. inset) The J (at 0.8 V) vs. t_{ox} performance of the STO films.[87]

The underlying electrode layer is prone to oxidation during the deposition of a dielectric layer and PDA. When the underlying TiN was oxidized (this is feasible even when the overlying noble metal layer remains intact due to the higher oxidation potential of Ti than Ru or Pt and the very thin layer thickness of Ru or Pt), the contact resistance between the capacitor and select transistor becomes too high or the conductivity of the electrode stack itself becomes too low to be used.[74]

The thin Pt layer catalyzes the oxidation of the underlying TiN layer so that oxidation of the TiN interface became even more serious than the oxidation of the bare TiN layer. The thin Ru (and also Ir) offered slight protection from oxidation.[92] In addition, there has been significant improvement in the MOCVD and ALD of Ru (and partly RuO_2) thin films over the past decade. Therefore, Ru and RuO_2 are the most feasible electrode materials when the noble metal layer should really be adopted.

MOCVD of the Ru layer was attempted using a range of precursors.[55,93–96] However, most are based on the oxidative decomposition of the MO Ru-precursor and subsequent reduction of the RuO_x layer. This is a feasible route for forming the noble metal layer because of the lower oxidation potential of RuO_2 compared to those of CO, CO_2 and H_2O.[97] However, they usually show somewhat poor nucleation behavior on most substrates including SiO_2 and TiN (or TiO_xN_y), which are the two materials over which the Ru layer was deposited.[58,98] Delayed nucleation normally resulted in a rougher surface morphology, which eventually degrades the dielectric performance of the high-ε dielectric layer on the top. This is apparently the case for Ru thin film growth by ALD,[99] where the chemical bonding type (ionic, covalent, or metallic) of the substrates surface play a key role in determining the initial nucleation delay. Ionic and metallic bonding generally favored the more fluent nucleation.[58,99] It was also reported that the supply of oxygen from a growing surface or sub-surface to chemically adsorbing Ru-precursor molecules is crucial to the ALD of Ru.[100] However, the authors recently reported that the catalytic dissociative adsorption of O_2 molecules do not play a role in nucleating the Ru layer on a metal surface.[101] **Figure 10a** shows the change in the Ru layer density on various substrates as a function of the number of ALD cycles when 2,4-(dimethylpentadienyl)(ethylcyclopentadienyl)Ru (DER) and O_2 were used as the Ru-precursor and reactant, respectively, at an ALD temperature of 250 °C. The more covalently bonded substrates (SiO_2 and TiN) showed the longest incubation cycles, whereas the metallic Pt and Au substrates showed almost negligible incubation cycles.[101] The ionic TiO_2 substrate showed an intermediate value. It should be noted that catalytic Pt and non-catalytic Au toward the dissociative adsorption of O_2 did not show any difference in growth behavior. The importance of this behavior is discussed in detail elsewhere.[101] Figure 10b shows the excellent step coverage of the Ru layer grown on the contact hole with an aspect ratio of 17 formed in the SiO_2 layer.

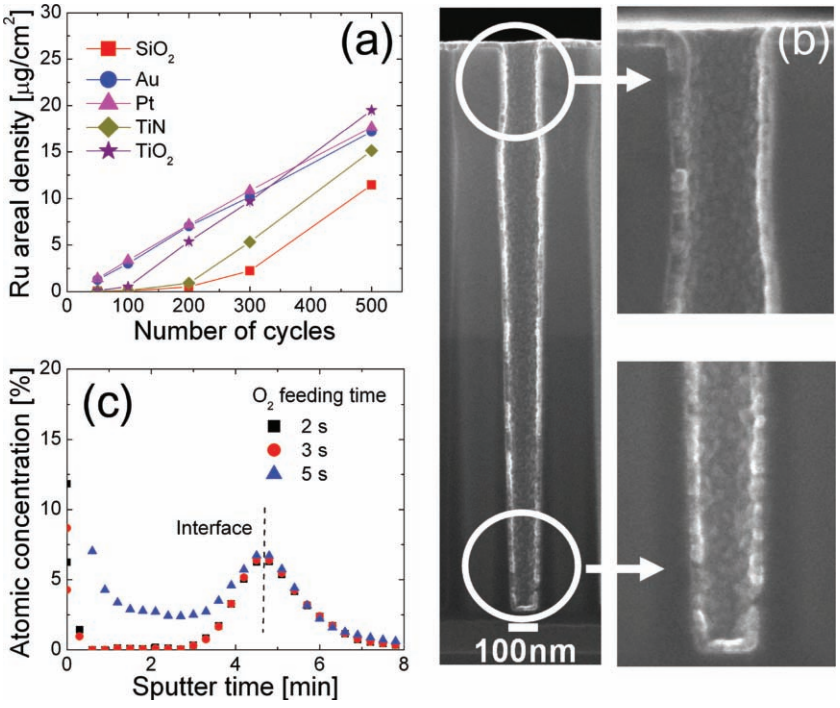

Figure 10. a) Change in the Ru layer density of Ru films on various substrates as a function of deposition cycles.[101] Reproduced with permission [101]. Copyright 2010, American Chemical Society. b) Cross-section SEM image of Ru film on the contact hole with an aspect ratio of 17.[99] Reproduced with permission [99]. Copyright 2007, American Institute of Physics. c) AES depth profile of oxygen concentration in the Ru films grown on native oxide/Si substrate.

The residual oxygen in the Ru film induces several problems, such as oxidation of the underlying TiN layer and agglomeration during the PDA. Figure 10c shows that the excessive oxygen pulse time (5 s) during ALD results in residual oxygen in the film. Meanwhile, the growth of stoichiometric RuO_2 is not feasible using a similar ALD process by simply increasing the O_2 pulse to a longer time because the oxidized RuO_2 layer is easily reduced during the subsequent MO precursor pulse step. Therefore, Kim et al. reported that a back ground flow of oxygen during the entire ALD steps is necessary to achieve a RuO_2 film by ALD.[102]

There is another approach for producing Ru thin films, where an inorganic RuO_4 precursor was adopted and reduced with the assistance of H_2 gas, which is in contrast to the oxidative deposition of MO Ru-precursors.[103,104] Although Gatineau et al. reported that ALD type growth is probable with this precursor,[104] it was recently reported that Ru film growth by this precursor was governed mainly by a CVD-type deposition mechanism, where the ALD-like source pulse–purge–reactant pulse–purge steps were repeated.[103] **Figure 11a** shows the changes in the Ru layer density as a function of the pulse-CVD (p-CVD) cycle number using the RuO_4 precursor and H_2 (5% in N_2 dilute gas) reduction gas at a growth temperature of 230 °C. Here, RuO_4 was dissolved in a methylethyl fluorinated solvent, vaporized at 3 °C and pulsed for 3 s. H_2 reduction gas was pulsed for 10 s. A higher growth

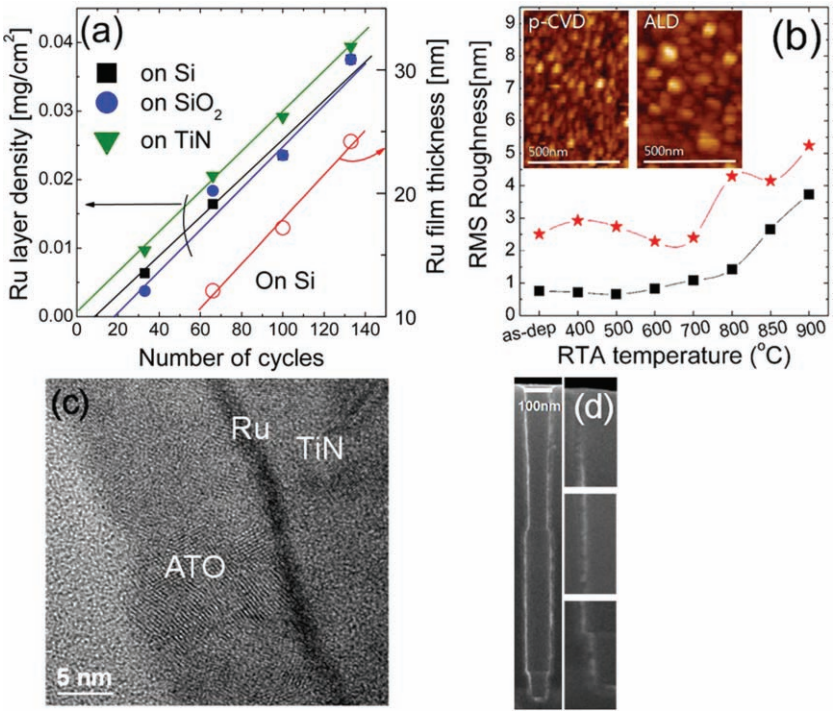

Figure 11. a) Variations in the Ru layer density of the films as a function of the number of cycles on various substrates.[103] Reproduced with permission [103]. Copyright 2009, American Chemical Society. b) Variation in the RMS roughness of 20 nm thick Ru films grown by p-CVD and ALD methods, respectively, as a function of RTA temperature.[103] Reproduced with permission [103]. Copyright 2009, American Chemical Society. c) TEM image of ATO/thin Ru layer grown from RuO_4/TiN stack.[105] d) Cross-section SEM image of p-CVD Ru film showing three-dimensional conformality on a hole structure with a opening diameter of 100 nm and a depth of 1000 nm.[103] Reproduced with permission [103]. Copyright 2009, American Chemical Society.

rate (0.18 nm per cycle) than the ALD process and a negligible incubation cycle were observed on the TiN substrate. This is in contrast to the ALD process with MO precursors.[99] The negligible incubation cycle suggests that nucleation was more fluent than the ALD process, which was confirmed in Figure 11b. The lower surface roughness of the as-deposited film by the p-CVD process using RuO_4 compared to the DER ALD process corroborates the more fluent nucleation, which was further confirmed by the AFM images in the inset. Furthermore, the p-CVD Ru films showed higher thermal stability due to the very low impurity concentration.[103] Interestingly, the oxygen concentration was even lower than that in the ALD films, suggesting the complete removal of oxygen by the H_2 reduction gas.[103] The highly uniform Ru film on the TiN substrate with a thickness as low as 2 nm (compare this with Figure 4c) was confirmed by high-resolution TEM (Figure 11c), where the ATO thin film was deposited on top of the p-CVD Ru/TiN layer.

There is some concern that CVD films generally have inferior step coverage to that of the ALD films. However, this is not the case here. The cross-section SEM image in Figure 11d shows highly conformal Ru layer growth by the p-CVD process over a severe 3D contact hole structure. This might be due to the high surface mobility of the adsorbed precursor molecules.

Figure 12 shows the GAXRD patterns of the 18 nm thick TiO_2 films on the TiN and Ru/TiN electrodes, where 1.6–8.0 nm thick Ru layers were grown on a non-plasma treated TiN layer by a p-CVD process. The TiO_2 layer on a Ru buffer layer, as thin as 1.6 nm, already shows a complete transition of its crystal structure from anatase (on TiN) to rutile. This is due to the very uniform growth of the Ru layer, even with such a small thickness, by this p-CVD process. More details on this will be reported elsewhere.[105]

As discussed in detail in section 2.2, the surface of a Ru layer is eventually oxidized in order for it to work as a suitable electrode for TiO_2 and ATO films. In addition, the STO/Ru interface has only a potential barrier height of ~0.5 eV, which is not high enough to suppress electron injection.[106] RuO_2 has a higher work function (~5.1 eV)[107] than Ru (4.7 eV). Therefore, RuO_2 may further improve the J–t_{ox} performance of STO films by decreasing the leakage current. As described previously, attempts have been made to form a thin, uniform and dense RuO_2 layer by a range of oxidation methods. However, the p-CVD of RuO_2 thin films was a much better method for achieving a better dielectric performance of a dielectric film grown on top through its smoother and denser structure. RuO_2 films were grown

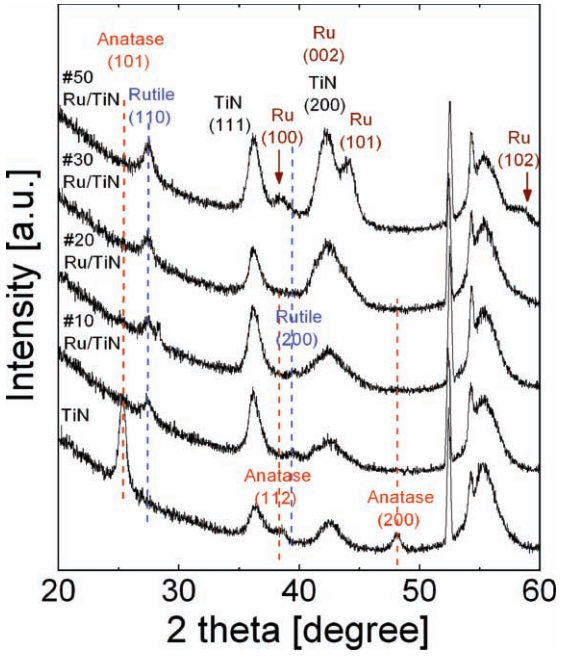

Figure 12. GAXRD patterns of TiO_2 films on TiN and 1.6, 3.2, 4.8, and 8 nm thick Ru/TiN substrates.

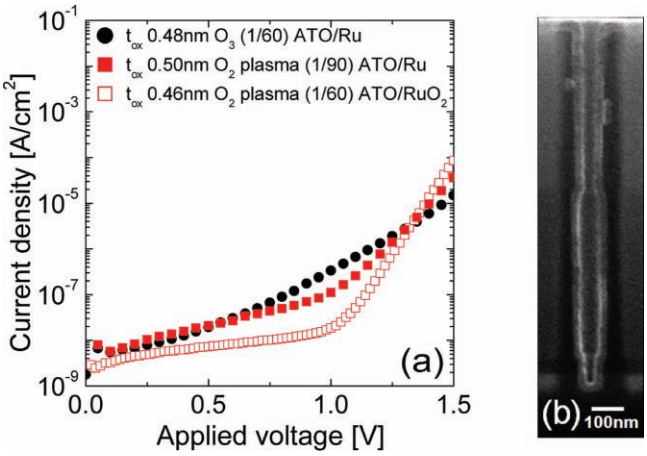

Figure 13. a) *J–V* curves of the ATO films with similar t_{ox} values grown on p-CVD Ru and RuO_2 electrodes by O_3-thermal ALD process and O_2 PEALD processes (1/60 and 1/90 stand for the Al/[Al±Ti] precursor feeding cycle ratio). b) Cross-section SEM image of p-CVD RuO_2 film grown on a SiO_2 hole structure with an aspect ratio of 10.

using the same p-CVD method with a shorter H_2 reduction gas pulse time (1–5 s). The details will be reported elsewhere.[108] **Figure 13a** shows the *J–V* curves of ATO films with similar t_{ox} values grown on sputtered Ru electrodes using the O_3-process (t_{ox} = 0.48 nm), on sputtered Ru electrodes using the O_2-plasma process (t_{ox} = 0.50 nm), and on p-CVD RuO_2 electrodes using the O_2-plasma process (t_{ox} = 0.46 nm). Even with the smaller t_{ox} value, the ATO films on the p-CVD RuO_2 electrode showed the smallest leakage current density (~1×10^{-8} A cm^{-2} at 0.8 V). This may be due to the RuO_2 layer having a very smooth surface morphology (RMS roughness ~1.73 nm at a thickness of 21.6 nm) and denser microstructure. The p-CVD RuO_2 film also showed highly conformal deposition behavior over the 3D contact hole structure, as shown in Figure 13b. Therefore, p-CVD RuO_2 is a promising material as the bottom electrode in a future DRAM capacitor. Further details on RuO_2 and dielectric films on RuO_2 electrode will be reported elsewhere.[108]

3. Concluding Remarks

This article reviewed the recent improvements in the fabrication of MIM capacitors, which may find applications in highly scaled DRAMs (<30 nm technology node). Perhaps perovskite STO (or (Ba,Sr)TiO_3) should be the ultimate material in present-style DRAM capacitors. However, the detrimental effect of the interface region on the overall dielectric performance, and the still immature process technology may hinder its easy adoption in the near term. In the mean time, TiO_2 or ATO may fill the technology gap between the preset ZAZ type dielectric and STO. Achieving rutile TiO_2 and ATO within a useful ALD window may be feasible due to local epitaxy between RuO_2 and TiO_2 (ATO also). The continuous and tremendous developments in processing technology with the advancements in precursor chemistry have been made over the past several years. The RuO_4-based p-CVD process of a Ru electrode (also RuO_2) on a TiN layer made the process more feasible as a mass-production compatible one. Currently, planar structured MIM capacitors with a laboratory scale experiment under a non-ideal environment confirmed that a minimum t_{ox} of ~0.46 nm can be achieved with a safe leakage current level. A similar minimum t_{ox} level was achieved using STO films. However, further t_{ox} scaling is expected due to the larger dielectric constant.

These improvements in the MIM capacitor technology might be used in other fields. The bulk-ceramic type multi layer ceramic capacitor is approaching its technical limit.[109] Applying thin film type MIM technology to this field must be a natural consequence, even though there are several technical challenges remaining.[110–112] Applying them to a supercapacitor for energy storage is another feasible area.[1,113]

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