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A detailed understanding of the electronic bipolar resistance switching behavior in Pt/TiO_2/Pt structure

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Abstract

The detailed mechanism of electronic bipolar resistance switching (BRS) in the Pt/TiO_2/Pt structure was examined. The conduction mechanism analysis showed that the trap-free and trap-mediated space-charge-limited conduction (SCLC) governs the low and high resistance state of BRS, respectively. The SCLC was confirmed by fitting the current–voltage characteristics of low and high resistance states at various temperatures. The BRS behavior originated from the asymmetric potential barrier for electrons escaping from, and trapping into, the trap sites with respect to the bias polarity. This asymmetric potential barrier was formed at the interface between the trap layer and trap-free layer. The detailed parameters such as trap density, and trap layer and trap-free layer thicknesses in the electronic BRS were evaluated. This showed that the degradation in the switching performance could be understood from the decrease and modified distribution of the trap densities in the trap layer.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

After the observation of voltage- (or current-) driven resistance switching phenomena in the 1960s, many types of oxide and non-oxide RS materials have been examined for their possible use in non-volatile semiconductor memory applications or reconfigurable logic circuits [1–3]. The newly found 'memristive' characteristics of the RS phenomena have given an extra push to the extensive study of RS behavior [4]. The various RS phenomena can be divided into unipolar resistance switching (URS) and bipolar resistance switching (BRS), where the set/reset switching bias polarity is the same for URS and different for BRS [5]. Although this classification is simple and clear, it barely gives any implications of the switching mechanism itself. Recently, Waser *et al* categorized the resistance switching behaviors into five types according to switching mechanism [6]. In this classification, the URS of oxide materials was newly defined as 'thermo-chemical type', where the formation and rupture of local conducting filaments cause the resistance switching. The other URS mechanism is the phase change type. The BRS is more complex and was categorized into three types, being electrostatic/electronic, electrochemical metallization and valence change types [6].

Among the various resistance switching materials available, simple binary oxide materials, such as TiO_2 [7] and NiO [8], could be better candidates than ternary or quaternary oxides for microelectronics applications because of their simpler fabrication process and compatibility with standard semiconductor technology. In particular, TiO_2 is an intriguing material where both URS and BRS are reported to occur concurrently [9]. The individually observed URS and BRS behaviors are well defined. The URS in TiO_2 was recently understood to originate from the formation and rupture of the Magnéli phase (Ti_nO_{2n-1}) conducting nanofilaments [10]. This is a typical example for resistance switching that belongs to the thermo-chemical group. Another well-defined BRS mechanism in TiO_2 is the valence change type BRS which is caused by the Schottky barrier height modulation that

comes from the movement of oxygen ions [11, 12]. A more detailed study showed that the valence change type BRS was observed in the metal/TiO_2/TiO_{2-x}/metal stacked structure ($x > 0$), where the Schottky barrier height of the metal/TiO_2 contact changed during resistance switching while the TiO_{2-x}/metal contact stayed ohmic [11]. Interestingly, the electrostatic/electronic type BRS, where the trapping and detrapping of electrons causes the resistance switching, could be responsible for the BRS in TiO_2 [13, 14]. Since the I–V characteristics of valence change and electronic types are similar, observing a clear distinction between them is not a trivial task. However, the electronic type BRS is an important switching mechanism, which is certainly distinctive from the valence change type one, shown not only in TiO_2 but also in many other oxide systems [15–18]. The electronic type BRS in TiO_2 was observed recently in the metal/TiO_{2-y}/TiO_{2-x}/metal stacked structure ($y > x > 0$) [19]. For this case, both electrode contacts remained ohmic which suggests that the Schottky barrier at the electrode/dielectric interfaces does not play a crucial role in the resistance switching. Instead, the layer with higher oxygen vacancy concentration (TiO_{2-y} layer) provided electron trapping sites and controlled the overall conductivity by trapping and detrapping [20]. Although the electronic type BRS in TiO_2 is an important switching mechanism, it has not been studied intensively compared to other mechanisms in TiO_2. In this paper, a detailed trap-mediated electronic type resistance switching behavior and its switching model in the Pt/TiO_2/Pt structure are presented.

2. Experimental procedure

A 60 nm thick TiO_2 thin film was deposited on a 100 nm thick sputtered Pt/SiO_2/Si substrate by plasma-enhanced atomic layer deposition at 250 °C using Ti-tetraisopropoxide and plasma-activated O_2 as the precursor and oxygen source, respectively. The TiO_2 film had a granular grain shape and the crystallographic structure was a mixture of anatase and brookite phases [10]. The possible presence of an amorphous phase cannot be excluded, and no specific preferred crystallographic orientation was found. More detailed results on structural analysis can be found in [10]. A 50 nm thick circular-shaped Pt top electrode (TE) with a diameter of 100 μm was then fabricated by electron beam evaporation followed by a photolithographic lift-off process. The resistive switching behavior of the films was measured at room temperature using an HP4145B semiconductor parameter analyzer. The switching behavior of the sample was measured by applying a bias voltage to the TE while the bottom electrode (BE) was grounded. For the conduction mechanism analysis in BRS, two samples were prepared. The first sample was an as-electroformed sample (sample A) where the initially insulating layer was electroformed to the low resistance state (LRS) by the I–V sweep with an appropriate current compliance and subsequently switched to the high resistance state (HRS) in URS mode. The HRS in URS mode is the state in which BRS is possible. Here, a positive bias voltage was applied to the TE during the URS. During the URS reset process, the metallic Magnéli phase filament was locally oxidized to oxygen-deficient TiO_2 (TiO_{2-x}), which is much more insulating than the filament, by a thermo-chemical reaction.

Since this filament rupture process is thermally driven, there must be an intermediate region (TiO_{2-y}) between the TE and TiO_{2-x}/residual filament where the oxygen vacancy concentration is higher than the TiO_{2-x} layer ($y > x$). This can be understood as follows; during the application of reset voltage to the TE, the oxygen ions are attracted to the TE side from the interior of TiO_2. Therefore, the filament region near the TE (which is the anode) is supposed to convert to an insulating phase. This is also because that part of the filament is weaker than the other part of the filament which means that the Joule heating effect is most effective in that region during the reset switching. However, it can also be anticipated that the filament region in the very vicinity of the TE may not be heated very efficiently due to the heat dissipation towards the TE. Therefore, it is probable that the reoxidation of the CF into the insulating phase is most efficient at a location slightly distant from the TE interface, which eventually results in the TE/TiO_{2-y}/TiO_{2-x}/residual filament/BE structure ($y > x$). This is schematically shown in figure 3(a). The details of this electroforming process can be found in [14]. As can be expected, the other parts of the sample remain inactive during the subsequent BRS due to their much higher resistances. Therefore, the changes in the electrical/electrostatic properties of these partially ruptured filament regions are focused on in this work.

The second sample was a degraded sample (sample B) where 100 times of switching were performed on sample A by using an Agilent 81110A current pulse generator. Here, −4 V, 50 ns and +4 V, 50 ns pulses were applied to the sample for set and reset switching, respectively. Although the switching voltage was <2 V in static I–V sweep mode, the pulse switching with short pulse duration required a higher voltage amplitude. During this switching condition, the switching endurance behavior deteriorated severely. The reason for this degradation will be discussed in section 3.4.

In order to better understand the electrical conduction behaviors of the various samples, the I–V curves of the LRS and HRS samples were measured at temperatures ranging from 40 to 90 °C.

3. Results and discussions

3.1. Space-charge-limited conduction in BRS

Figures 1(a) and (b) show the representative bipolar I–V sweep curves of samples A and B, respectively. The on/off current ratio of each sample was ∼20 (at 0.1 V) and ∼4 (at 0.1 V). In order to understand the switching mechanism for these cases, the fitting of the I–V curves with various electrical conduction mechanisms was attempted. It was found that the conduction mechanism of LRS and HRS fit well to the space-charge-limited conduction (SCLC) mechanism. Other conduction mechanisms such as Schottky, Poole–Frenkel and Fowler–Nordheim were investigated but they did not fit the I–V curves at all. Figures 1(c) and (d) show the fitting results

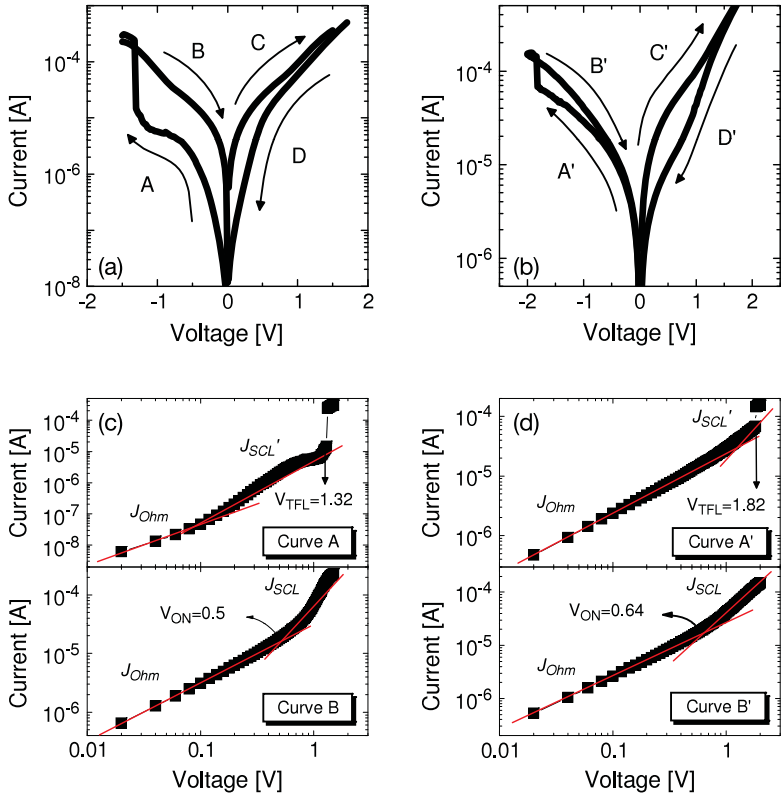

Figure 1. The BRS I–V curves which were acquired from (a) sample immediately after the electroforming and (b) sample after the switching performance degradation. The SCLC fit results of (c) curve A (upper panel) and curve B (lower panel) of (a), and (d) curve A′ (upper panel) and curve B′ (lower panel) of (b).

of curves A and B in figure 1(a) and curves A′ and B′ in figure 1(b), respectively, according to the SCLC theory. The SCLC mechanism is generally observed when the electrode contacts are highly carrier injecting [20]. Therefore, the residual Magnéli filament/Pt interface maintains quasi-ohmic properties, which is quite reasonable considering the metallic nature of the Magnéli phase near room temperature. Curves A and B of figure 1(a) (or curves A′ and B′ of figure 1(b)) fit well for the SCLC model with shallow traps and the trap-free SCLC model, respectively. Curves C and D (or curve C′ or D′) also show SCLC-like behavior in the low voltage ($\lesssim$1 V) regions but deviate from the model in the high voltage region, possibly due to the partial loss of trapped electrons (fitting data not shown). In the case of valence change type BRS, Schottky-type conduction must govern the overall current. The fact that both LRS and HRS follow SCLC means that the conduction is not governed by the interface barrier. This is prominent evidence of electronic type BRS for this specific type of electroformed and URS reset device [13]. The temperature dependence of the I–V curves also confirms the SCLC mechanism. In figures 2(a) and (b), the temperature-dependent (40–90 °C) log I–log V curves of the HRS and LRS samples, respectively, are shown. Since the repeated set/reset operations disturb the physical state of a given defect configuration, the temperature dependence was measured in the following way; the sample was made to be in the HRS by a positive reset pulse application. Then the I–V curves of the HRS were measured at various temperatures in negative voltage regions low enough to prevent the set operation. These measurements confirmed the SCLC mechanism in the HRS. Then, the sample was set to the LRS by applying a negative set I–V sweep, and the I–V curves were measured again at various temperatures to check the SCLC mechanism for the LRS. Here, the measurement voltage was limited from 0 V to −0.4 V and from 0 V to −1.0 V for the LRS and HRS, respectively, to inhibit reset and set switching during the measurements.

The LRS shows an ohmic behavior with a negligible temperature dependence in the whole voltage range. In contrast, the HRS also shows an ohmic behavior when small amounts of voltage are applied (0 to −0.2 V), but with a notable temperature dependence. As the voltage decreases further, the temperature dependence disappears and the I–V curve becomes clearly nonlinear. The I–V results for the LRS and HRS are plotted again in the Ln I versus $1000/T$ form at the given voltages as shown in figures 2(c) and (d). Each plot shows a generally straight line. From the slopes of the fitted lines, activation energies (E_a) were calculated at each voltage. Figure 2(e) shows the variation in calculated E_a of each state as a function of the voltage. They are generally small (0.02–0.03 eV for LRS and ∼0.04 eV for HRS, which are comparable to the thermal energy at room temperature) except for the near-zero voltage region (0 to −0.3 V) for HRS, where E_a reaches 0.25 eV at −0.1 V.

The absence of current decrease in both LRS and HRS with increasing temperature suggests that the conduction for both cases is not metallic although the I–V curves are linear

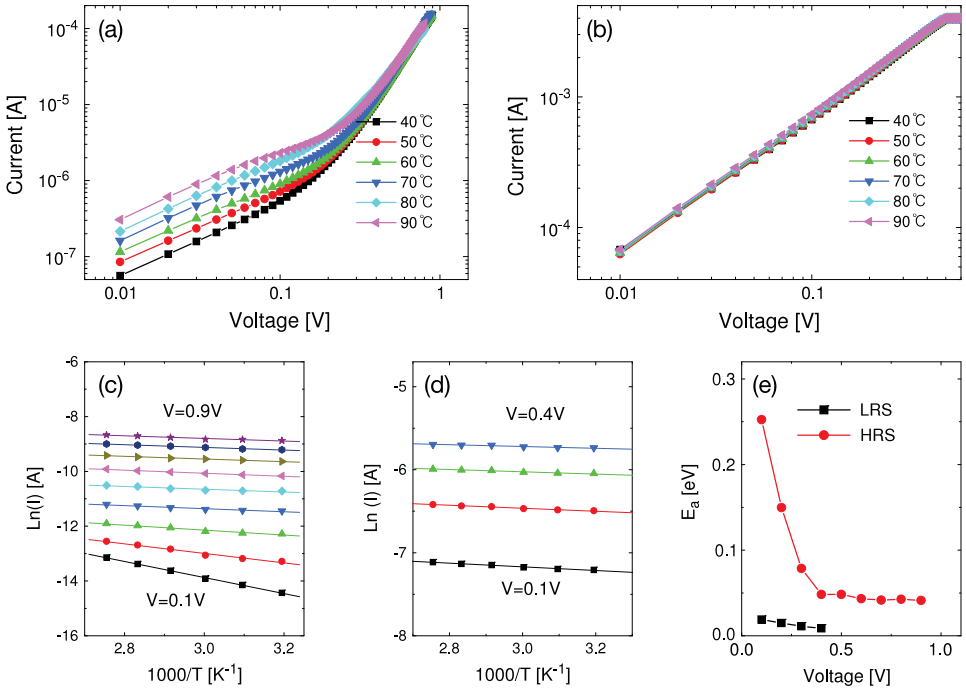

Figure 2. The log I–log V curves of the (a) HRS and (b) LRS, respectively, at measurement temperatures ranging from 40 to 90 °C. The Ln I versus $1000/T$ curves of the (c) HRS and (d) LRS at the given V. (e) shows the variations in the activation energy calculated from the slopes of the best linear fitted graphs of (c) and (d) as a function of V.

in the whole voltage region for LRS and in the high absolute voltage region (−0.3 to −1 V) for HRS. Therefore, the only feasible conduction mechanism in such a wide voltage range is SCLC. As can be understood from equations (1) and (2) shown later, SCLC has only a very weak temperature dependence due to the possible temperature dependence of electron mobility in the conduction band. For the near-zero voltage region (0 to −0.3 V) in HRS, the carrier concentration is not influenced by the weak carrier injection and ohmic conduction is observed. Under this circumstance, most of the carriers are trapped at the trap sites and hop to neighboring sites under voltage application. The hopping conduction mechanism in the small voltage region shows a linear I–V characteristic [20]. The non-negligible activation energy (∼0.25 eV@−0.1 V) for this voltage region may correspond to the E_a of this hopping process. This is in good agreement with the energy level of deep traps in TiO_2 [21–23] and the E_a obtained by impedance measurement [13]. As the absolute voltage increases in HRS, the I–V curves deviate from linear behavior because of the larger current injection. As the injected electrons fill up the trap sites, electrons begin to jump into the conduction band. Therefore, the HRS-to-LRS switching occurs as the electrons in the conduction band move freely with negligible E_a.

3.2. A model for the electronic bipolar switching

Electronic type BRS corresponds to a case where the trap-mediated hysteretic electronic conduction is asymmetric with respect to the bias polarity. This can be achieved after an electroforming process from TiO_2 film in this study. Figures 3(a) and (b) show schematic diagrams of the LRS and HRS of TiO_2, respectively, in electronic BRS mode. Here, the TiO_2 was divided schematically into the switching region, where the filament ruptured, and the filament region (the top panels of figure 3). The filament region can be regarded as an electrode forming an ohmic contact. The authors reported recently that such a situation can be readily achieved when the Magnéli phase filament ruptures near the anode interface [10]. In that report, the switching region can be divided into two layers, one being the switching layer (TiO_{2-y}), where the resistance switching occur, and the other being the non-switching layer (TiO_{2-x}) which is inevitable for resistance switching even though no switching occurs (see the bottom panels of figure 3). The switching layer contains a much higher density of electron traps (probably oxygen vacancies) causing the resistance change by the trapping and detrapping of electrons. Due to this reason, the switching layer and non-switching layer can be specified to be the trap layer and trap-free layer, respectively. In this structure, the switching region controls the electrical conduction as shown below.

The presence of bulk traps in the switching region has a significant influence on carrier transport [20]. In the HRS, the trap centers are empty which allows them to capture charge carriers. However, if the trapping centers are already filled with electrons during the previous set pulse step or voltage sweep, the conducting electrons are not influenced by the traps, resulting in an LRS. Therefore, current conduction through the trap-mediated SCLC mechanism can be intrinsically hysteretic only if the detrapping of the carriers is not activated by thermal energy. On the other hand, regaining the HRS requires the detrapping of trapped carriers through electronic means. This can be realized by the presence of an asymmetric potential

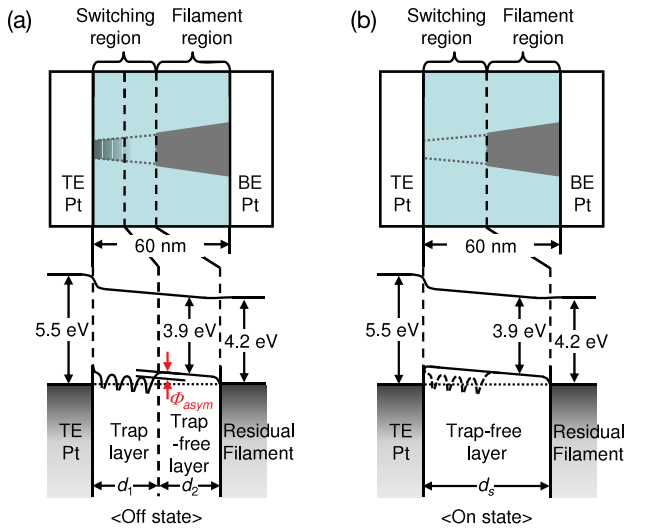

Figure 3. The upper panels show the schematic diagram of (a) HRS and (b) LRS in top electrode Pt/TiO_{2-y}/TiO_{2-x}/residual filament structure. The solid conical shape of (a) and (b) represents the residual filaments. The gradient of shading at the TE Pt side of (a) represents the supposed trap distribution; the higher the trap density is, the darker the region. A conical filament is supposed with a gray color. The lower panels show the corresponding band diagrams of the switching region.

barrier of traps (Φ_{asym}) with respect to bias direction, as shown in figure 3(a). The rationale for the presence of Φ_{asym} can be found from the calculated trap density, as shown in section 3.3.

When a negative bias was applied to the HRS, the injected electrons from the top electrode are easily trapped due to the presence of Φ_{asym}. At the trap filling limit voltage (V_{TFL} or V_{set}^{B}, ~−1.4 V), all the traps are filled with electrons and a sudden current jump which corresponds to set switching is observed (curves A and A′ of figure 1). It should be noted that the trapped electrons are not easily detrapped with increasing negative bias after set switching occurs or even when positive bias is applied to the top electrode, on the condition that the positive voltage is less than the reset threshold voltage (V_{th}), which is ~0.5 V in figure 1, due to the significant depth of the trap level. In TiO_2, the trap depth was reported to be from ~0.8 eV [21] to ~1 eV [22, 23]. Hence, the trap depth shown in figure 3 can be as high as 0.7–0.8 eV. Therefore, since the traps are still filled with electrons, an LRS current is maintained under the negative (curves B and B′) and positive bias (curves C and C′ below 0.5 V). Once the positive bias reaches V_{th}, trapped electrons start to escape to the top electrode, resulting in a bipolar HRS (curves D and D′). This is because Φ_{asym} does not act against the detrapping process under a positive bias.

3.3. Estimation of the thicknesses of the trap layer and trap-free layer

The thicknesses of the trap layer (d_1) and trap-free layer (d_2) and trap densities (N_t) in the trap layer can be obtained by fitting the experimental I–V curves with a double-layer model. For this fitting, the discrete trap distributions of the two layers and the voltage distribution over the two layers were considered. There should be some gradual change in the trap density along the direction normal to the interface within the switching region in figure 3. However, a discrete two-layer trap distribution is assumed for the sake of simplicity. The regions between the ruptured filaments (non-filament region) are assumed to be much more insulating and not to contribute to the BRS. However, there are quite a large number of ruptured (or incomplete) filaments in the sample, so the local regions where the BRS occurs take an integral part of the sample volume, and sometimes they can even overlap. This could be the basic reason for the area-dependent resistance of the LRS and HRS in electronic type BRS (data not shown). Therefore, in this work, the traps are assumed to be uniformly distributed over the sample surface area. In the following section, the I–V curves were analyzed according to the relative trapped carrier density (n_t) compared to the free carrier density (n).

3.3.1. When n_t is much larger than n. This case corresponds to the I–V curves of sample A as shown in figure 1(a) where a high trap density is present in the trap layer. First, trap-free SCLC is considered to understand the LRS I–V curves such as curve B in figure 1(a). In this case, all the traps are already filled with carriers so there is no difference between the trap layer (d_1) and trap-free layer (d_2), as shown in figure 3(b). This means that the trap-free layer thickness is simply the switching region thickness (d_s). In trap-free SCLC, the ohmic current density (J_{Ohm}), trap-free SCL current density (J_{SCL}) and ohmic to SCLC transition voltage (V_{ON}) are given as follows [20]:

$$J_{Ohm} = qn_0\mu_n\frac{V}{d_s} \tag{1}$$

$$J_{SCL} = \frac{9}{8}\varepsilon_o\varepsilon_r\mu_n\frac{V^2}{d_s^3} \tag{2}$$

$$V_{ON} = \frac{8}{9}\frac{qn_0d_s^2}{\varepsilon_o\varepsilon_r}, \tag{3}$$

where q is the elementary charge, μ_n is the electron mobility in the TiO_2 film (this was assumed to be ~10^{-6} $cm^2\,V^{-1}\,s^{-1}$ [24], see below), n_0 is the thermally produced free carrier density, ε_r is the low frequency dielectric constant of TiO_2 ($\varepsilon_r \cong 40$ in anatase TiO_2 [25]) and ε_o is the vacuum permittivity. The values of μ_n found in the literature vary widely from 8 $cm^2\,V^{-1}\,s^{-1}$ for single-crystalline rutile [26] to 10^{-6} $cm^2\,V^{-1}\,s^{-1}$ for non-stoichiometric polycrystalline anatase with relatively low density [24]. Considering the heavily damaged microstructure and higher defect density of the switching region [10], the lower value of μ_n was used in this calculation. By fitting curve B in figure 1(c) to equations (1) and (3), d_s and n_0 were determined to be 19.3 nm and 3.34×10^{18} cm^{-3}, respectively. It is noted that d_s is approximately only half of the total thickness of the TiO_2 film, confirming that the schematic structure in figure 3 is reasonable. This is also consistent with the earlier report made by the authors [27] although the d_s in this calculation is slightly larger.

Secondly, curve A in figure 1(a), which corresponds to the HRS by the presence of empty traps, was considered. Here,

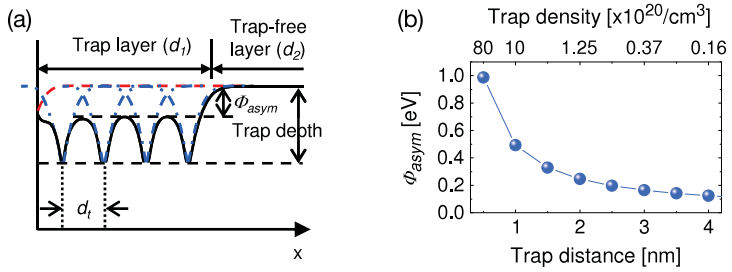

Figure 4. (a) The energy band structure considering the Coulombic interactions between the free carrier and trap centers (blue dotted–dashed line) and the image force effect (red dashed line). (b) The barrier lowering (Φ_{asym}) as a function of the trap distance or trap density.

the traps are assumed to have a single discrete energy level, which is determined by the vacancy level in the energy gap. In addition, the traps have a spatial distribution within d_s (d_1 and d_2 layers). In this case, the SCL current can be expressed as follows [20]:

$$J_{SCL} = \frac{9}{8}\varepsilon_o\varepsilon_r\mu_n\theta_a\frac{V^2}{d_{eff}^3}, \tag{4}$$

where $\theta_a = n/(n + n_t)$, which is 0.061 in this case, is the measured current ratio before and after the current jump at V_{TFL}, and

$$d_{eff} = \left\{\frac{3}{2}\int_0^d\left(\int_0^t [\theta_a + S(x)]\,dx\right)^{1/2}dt\right\}^{2/3}, \tag{5}$$

where $S(x)$ represents the spatial distribution. By assuming the double-layer model for trap distribution, the spatial distribution can be expressed simply as

$$S(x) = \begin{cases} 1-\theta_a & (0 < x < d_1) \\ 0 & (d_1 < x < d_s). \end{cases} \tag{6}$$

Equation (6) suggests that the carrier density in the d_2 layer is $\theta_a \times$ (the total carrier density in d_1 layer). The difference between d_s and d_{eff} can be attributed to the inhomogeneous spatial distribution of free and trapped carriers. Since the trapped carrier density is much higher than the free carrier density, the integral in equation (5) within the trap-free layer ($d_1 < x < d_s$) is negligible. Thus, d_{eff} can be approximated to the trap layer thickness ($d_{eff} \sim d_1$). This means that the overall conduction is governed by the trap layer (d_1). By fitting curve A to equation (4) for a given θ_a (figure 1(c)), d_{eff} was determined to be 6.1 nm.

The total trap density (N_t) in the trap region (d_1) can be calculated as follows. In SCLC with shallow traps, V_{TFL} is given as equation (7) [20]:

$$V_{TFL} = \frac{q(n + N_t)d_1^2}{2\varepsilon_o\varepsilon_r}. \tag{7}$$

Here, the measured V_{TFL} was applied over the whole switching layer (d_s). Therefore, the actual V_{TFL} applied to the d_1 layer needs to be calculated from the resistance ratio of d_1 and d_2. Because of the much higher resistance of the d_1 layer compared to d_2, it can be assumed that all of the measured V_{TFL} was applied to the d_1 layer. As a result, $(n + N_t) = 1.57 \times 10^{20}$ cm^{-3} according to equation (7). Here, n is the free carrier density (mainly comprised of injected carriers). Because $\theta_a = 0.061$, n and n_t are 9.58×10^{18} and 1.48×10^{20} cm^{-3}, respectively, at V_{TFL} ($N_t = n_t$), where n_t is the trapped carrier density. With this N_t, the average distance between traps (d_t) is 1.9 nm ($d_t = N_t^{-1/3}$) assuming that the traps are distributed uniformly within d_1. This N_t value is high enough to induce SCLC and decrease the local Schottky barrier height with the Pt electrode (see figure 4). The high N_t makes the Schottky barrier width thin enough for electrons to tunnel through. In addition, the first-principles calculation revealed that the accumulation of oxygen vacancies at the metal/titanate interface largely reduces the Schottky barrier height [28, 29].

3.3.2. When n_t is ∼n. In this experiment, it was assumed that the distribution of ionic defects or traps (mainly oxygen vacancies) is invariant for a single cycle, and that the electrons fill or empty these traps according to bias voltage. This type of configuration of traps is assumed to be favorable for such electronic type BRS to occur. In practice, however, the distribution of defects must be slightly changed even after a single cycle. The slight changes could be accumulated as the switching proceeds, so that this may not be the case after the repeated switching cycles. Since the switching region has an exceptionally high vacancy concentration, which is thermodynamically unfavorable, the repeated switching operations may cure the vacancies. This could be further supported by the Joule heat produced during the switching experiment. Therefore, the overall trap density in the trap region could be reduced as the number of cycles increases. This is discussed again in the later part of this section. This case corresponds to the I–V curves of sample B as shown in figure 1(b).

For trap-free SCLC, d_s and n_0 could be calculated by the same method as shown in section 3.3.1. By fitting curve B′ to equations (1) and (3) (figure 1(d)), d_s and n_0 were determined to be 19.7 nm and 4.11×10^{18} cm^{-3}, respectively, which are very similar to those in sample A. This means the status of the switching region (overall thickness and free carrier density) in the LRS was not changed much although the switching performance of the sample was degraded severely. However, there is a large variation in the d_1 to d_2 layer thickness ratio and N_t.

Then, curve A′ in figure 1(b) was considered. In this curve, θ_a was calculated to be 0.48 and thus the trap-free layer was

not negligible any more. By fitting curve A′ in figure 1(b) to equation (4) for the given θ_a, d_{eff} was determined to be 19.1 nm, which was slightly smaller than d_{s} (19.7 nm). It needs to be remembered that, when $\theta_a \sim 0$, d_{eff} was approximated to the trap layer thickness (d_1) as shown in section 3.3.1. However, in this case, where $\theta_a = 0.48$, the trap-free layer thickness should also be included in d_{eff}. From equations (5) and (6), and $d_{\text{s}} = d_1 + d_2$, d_1 and d_2 were calculated to be 18.5 and 1.2 nm, respectively.

The total trap density (N_{t}) in the trap region (d_1) was also evaluated. Due to the thicker thickness and higher resistance of the d_1 layer, almost all of the V_{TFL} in curve A′ (1.82 V) was applied to the d_1 layer. Then, $(n + N_{\text{t}}) = 2.35 \times 10^{19}$ cm^{-3} according to equation (7). Because $\theta_a = 0.48$, n and n_{t} were 1.13×10^{19} and 1.22×10^{19} cm^{-3}, respectively, at V_{TFL} ($N_{\text{t}} = n_{\text{t}}$). With this N_{t}, the d_{t} was 4.3 nm assuming that the traps show a uniform distribution in d_1. Therefore, it can be understood that the trapped carrier density decreases by almost one order of magnitude after 100 cycles. This caused the smaller resistance ratio of sample B compared to that of sample A.

3.4. Estimation of the asymmetric trap barrier height (Φ_{asym})

The height of the asymmetric trap barrier (Φ_{asym}) in figure 3(a) can be estimated from the fitted values for d_1 and d_{t} by the following procedure. The image charges in the electrode and the Coulombic interaction between the free carrier and trap centers were considered for the estimation. Figure 4(a) represents a detailed energy profile around the traps. Barrier lowering at the metal–insulator interface by image charges is well described as follows [20];

$$E_i(x) = \frac{q^2}{16\pi\varepsilon_h x}, \tag{8}$$

where x is the depth from the metal–insulator interface shown in figure 4(a) and ε_h is the optical frequency dielectric constant. This is shown as the red dashed line in figure 4(a). Barrier lowering by the Coulombic interaction between the traps is given as follows;

$$E_{\text{t}}(x) = \sum_n \frac{q^2}{4\pi\varepsilon_l |(x - nd_{\text{t}})|}, \tag{9}$$

where ε_l is the static dielectric constant. This is shown as the blue dotted–dashed line in figure 4(a). Then, the total barrier lowering is the sum of these two terms and is shown as the black line in figure 4(a). In the cases of the I–V curves shown in figures 1(a) and (b), Φ_{asym} was calculated to be ∼0.26 eV ($d_{\text{t}} = 1.9$ nm) and ∼0.10 eV ($d_{\text{t}} = 4.3$ nm), respectively. Figure 4(b) shows the change in Φ_{asym} as a function of d_{t} and N_{t}. Φ_{asym} increases with increasing N_{t}, which corresponds to the more hysteretic I–V curves with higher on/off current ratios. In passing, the actual Φ_{asym} must be slightly larger than 0.26 and 0.1 eV because the N_{t} must be slightly higher than the calculated values here as they were assumed to be uniformly distributed over all the surface area. In actual cases they should be a little more localized near the remaining CF region.

From the I–V fitting results of samples A and B, it was found that the degradation in the on/off resistance ratio with the increasing number of switchings originated from the variations in the density and distribution of traps in d_{s}. In sample A, the trap density was higher (1.48×10^{20} cm^{-3}) and the trap layer thickness was small (6.1 nm). In sample B, where the switching performance was degraded, the trap density was reduced to 1.22×10^{19} cm^{-3} but the trap layer thickness was increased to 18.5 nm. This suggests that the total number of traps ($n_{\text{t}} \times d_1$) in the trap layer was decreased from 9.03×10^{13} to 2.26×10^{13} cm^{-2} after the repeated switching. This means that the repeated bipolar switching removed some traps and rearranged the distribution over a thicker thickness. The repeated application of opposite bias voltages for the set/reset switching inevitably induced an alternating movement of oxygen ions, which degrades the switching performance, as well as the hysteretic electron trapping/detrapping. This oxygen ion movement is governed by the electric field as well as the thermal energy produced by the Joule heating effect. For the given asymmetric I–V curves with respect to the bias voltage, it is quite natural to expect an imbalanced back-and-forth movement of oxygen ions, which eventually modifies the trap density and configuration. This is rather inconvenient for electronic type BRS and a method that can improve this problem will be reported elsewhere.

From the presence of Φ_{asym} and deep traps, the BRS in this work can be qualitatively understood as follows. After the electroforming or URS reset operation, the switching region, which is actually composed of two layers, d_1 and d_2, is formed near the top Pt interface in this case. The d_1 layer contains a high density of traps while the d_2 layer is devoid of them. There is Φ_{asym} between the two, of which the magnitude is 0.2–0.3 eV. The trap depth from the original conduction band must be ∼1 eV, so the trap depth from the pseudo-continuous conduction band edge is 0.7–0.8 eV. This trap depth is deep enough to hold the electrons against the thermal energy of the trapped electrons. When a negative bias was applied to the top Pt electrode, electrons were injected and trapped until all the traps were filled with injected electrons. Then at V_{TFL} the influence of the traps disappears and the current jumps, achieving the LRS. This corresponds to curves A and A′ in figures 1(a) and (b). During this operation, the Φ_{asym} works as a barrier for the electrons to flow into the counter electrode (in this case it is the residual filament) which generally enhances the electron trapping, so the switching from the HRS to LRS is generally observed. In the subsequent application of negative bias but with smaller magnitude (curves B and B′ in figures 1(a) and (b)) this trap-filled state was maintained and the LRS was retained. This state was further retained even under the positive bias up to a certain level (low V region of curves C and C′ in figures 1(a) and (b)). However, when the positive bias was increased to a sufficiently larger value, the trapped electrons were drained off to the TE. The Φ_{asym} does not play a role against this action. In addition, the slightly high Schottky barrier at the d_2 layer/residual filament interface does not allow the fluent injection of electrons into the trap region through the d_2 layer. Following the removal of the trapped electrons, the HRS was recovered as shown by curves D and D′ and also A and A′ in figures 1(a) and (b).

4. Conclusion

In this work, an electronic type BRS behavior observed in the Pt/TiO_2/Pt structure was analyzed. The fitting of I–V curves and temperature-dependent I–V measurements showed that the trap-mediated and trap-free SCLC controlled the conduction of HRS and LRS, respectively. Complying with this result, a discrete double-layer (trap layer/trap-free layer) structure of the switching layer was suggested, and the values of each layer thickness and trap density were evaluated from the SCLC I–V results for the cases of a fresh sample and a degraded sample. The asymmetric potential barrier of the trap sites, originating from the non-uniform special distribution of electron trap centers, causes a bias-polarity-dependent electron trapping and detrapping behavior. In the fresh sample, the oxygen vacancy concentration is as high as $\sim 1.48 \times 10^{20}$ cm^{-3} within the 6.1 nm thick layer at the anode interface. In the degraded sample, the trap density ($\sim 1.22 \times 10^{19}$ cm^{-3}) and trap layer thickness (18.5 nm) became smaller and broader. It was shown that the switching performance degradation is caused by the spreading out of traps from the trap layer to the trap-free layer. The presence of the asymmetric potential barrier between the trap layer and trap-free layer, and the deep trap level within the trap layer constitute the reasons for the presence of the hysteretic I–V curves. In principle, electronic type BRS does not involve, although the actual situation is quite complicated, the motion of ionic defects once the optimal distribution of them is established, and is dependent only on electronic motion. Therefore, electronic type BRS can be a strong contender for resistive switching memory with higher reliability compared to valence change type BRS.

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